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ERTEC 200P-3

Enhanced Real-Time Ethernet Controller

Data Sheet

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We have reviewed the contents of this publication to ensure consistency with the hardware and software described. Since variance cannot be precluded entirely, we cannot guarantee full consistency. However, the information in this publication is reviewed regularly and any necessary corrections are included in subsequent editions. Suggestions for improvement are welcome.

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Preface

Target audience of this data sheet

This data sheet is intended for hardware and software developers who want to use the ERTEC 200P-3 for new products. Experience working with processors and designing embedded systems and knowledge of Ethernet are required for this.

The data sheet describes the ERTEC function groups in detail and provides information that you must take into account when configuring your own PROFINET IO device hardware.

The data sheet serves as a reference for hardware and software developers. The address areas and register contents are described in detail for the function groups.

Scope of the data sheet

This data sheet is valid only for ERTEC 200P-3. For information on ERTEC 200P-1/2, refer to the respective data sheet.

Guide

To help you quickly find the information you need, this data sheet contains the following aids:

A complete table of contents as well as a list of figures and tables in the data sheet are provided at the beginning of the data sheet, followed by a list of abbrevations used in the data sheet.

Conventions

ERTEC 200P, ERTEC 200P-3: We refer to “ERTEC 200P“ or "ERTEC 200P-3" in this documentation as a synonym for ERTEC 200P Step3.

This documentation contains pictures of the devices described. The figures may differ slightly from the device supplied.

You should also pay particular attention to notes such as the one shown below:

Note

A note contains important information on the product, on handling of the product and on the section of the documentation to which you should pay particular attention.

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Technical Support

Technical information and support on development packages are provided by Support Team:

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PROFINET Certification

Comprehensive consulting prior to starting the development project is particularly important for an efficient and successful development process. The final step in field device development is certification. For PROFINET, Siemens also offers you independent, accredited test laboratories like “ComDeC” in Germany, “PIC” in the USA, “ITEI” in China, and “an testlabs” in the Czech Republic.

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Overview

- **Integrated processor ARM926EJ-S**
  - 250 MHz Core Frequency
  - 16 KByte Data-Cache
  - 16 KByte Instruction-Cache
  - 256 KByte TCM
  - 8 KByte Boot ROM
  - Little-endian

- **System Bus Structure**
  - 32 Bit / 125 MHz AHB Bus
  - Multi-Layer AHB Lite with 9 Masters and 18 Slaves
  - AHB Address Range Monitoring
  - Round Robin or Fixed Priority

- **Local Bus Unit (XHIF)**
  - Allows External Master to access internal ERTEC 200P-3 registers
  - 16 / 32-Bit Data Bus
  - 2 x 4 Paging Registers

- **Memory Controller (EMC)**
  - 8 / 16 / 32 Bit Data Bus
  - 4 chip selects
  - supports SDRAM, SRAM

- **Onchip Peripherals**
  - DMA Controller
  - 6 Timers
  - 2 Watchdogs

- **I/O Interfaces**
  - 1 Octal SPI Interface
  - 2 x 2 SPI Interfaces
  - 4 UARTs
  - 1 I²C-Interface
  - One 96-bit GPIO Port
  - 1.8 / 3.3 V I/O Buffers

- **Test / Debug Functionality**
  - Boundary Scan
  - EJTAG for Debugging

- **Integrated Ethernet-Phy**
  - 2 Ports
  - Supports 100BASE-TX and -FX
  - Auto Cross Over
  - Auto MDIX
  - Jitter free Latency

- **Package**
  - 358 Pin P-LFBGA
  - Size 17 x 17 mm
  - Ball Pitch 0.8mm

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Table of Contents

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List of Figures

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List of Tables

Abbreviations

Abbreviation	Description
AHB	AMBA **A**dvanced **H**igh-performance **B**us
AMBA	**A**dvanced **M**icrocontroller **B**us **A**rchitecture
APB	AMBA **A**dvanced **P**eripheral **B**us
CAS	**C**olumn **A**ddress **S**ignal
CR	**C**ommunication **R**elationship (e.g. input data / output data)
CRU	**C**lock **R**eset **U**nit
DMA	**D**irect **M**emroy **A**ccess
DP	**D**istributed **P**eripherals
ECC	**E**rror **C**orrection **C**ode
EMC	**E**xternal **M**emory **C**ontroller
ENC	**Enc**oder Interface
ETB	**E**mbedded **T**race **B**uffer
ETM	**E**mbedded **T**race **M**acrocell
FIFO	**F**irst **I**n **F**irst **O**ut
FIT	**F**ailure **I**n **T**ime
GDMA	**G**eneric **D**irect **M**emory **A**ccess
GPIO	**G**eneral **P**urpose **I**nput/**O**utput

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Abbreviation	Description
HW	**H**ard**w**are / **H**alf-**W**ord
HWAL	**H**ard**w**are **A**bstraction **L**ayer
ICE	**I**n **C**ircuit **E**mulation
ICU	**I**nterrupt **C**ontrol **U**nit
IP	Intellectual Property
IRQ	**I**nterrupt **Req**uest
IRT	**I**sochronous **R**eal **T**ime
JTAG	**J**oint **T**est **A**ction **G**roup
LVPECL	**L**ow-**V**oltag **P**ositive **E**mitter **C**oupled **L**ogic
MC	**M**otion **C**ontrol
MMD	**M**emory **M**ap **D**ecoder
MMU	**M**emory **M**anagement **U**nit
n.a.	**n**ot **a**pplicable
PCB	**P**rinted **C**ircuit **B**oard
PCI	**P**eripheral **C**ommunication **I**nterface
PECL	**P**ositive **E**mitter **C**oupled **L**ogic
PHY	**Phy**sical Layer
PLL	**P**hase **L**ocked **L**oop
PNPLL	**P**ROF**IN**ET **PLL**
PRBS	**P**seudo **R**andom **B**inary **S**equence
PTCP	**P**recision **T**ransparent **C**lock **P**rotocol
RAS	**R**ow **A**ddress **S**ignal
RD	**R**ead
SCRB	**S**ystem **C**ontrol **R**egister **B**lock
SDRAM	**S**ynchronous **D**ynamic **RAM**
SMI	**S**erial **M**anagement **I**nterface
SMT	**S**erial **M**odule **T**est
SPI	**S**erial **P**eripheral **I**nterface
SRAM	**S**tatic **R**andom **A**ccess **M**emory
SW	**S**oft**w**are
TCM	**T**ightly **C**oupled **M**emory
TLB	**T**ranslation **L**ookaside **B**uffers
UART	**U**niversal **A**synchronous **R**eceiver**/**Transmitter
UTP	**U**nshielded **T**wisted **P**air

Abbreviation	Description
W	**W**ord
WR	**W**rite

1 Functional Overview

1.1 Block diagram

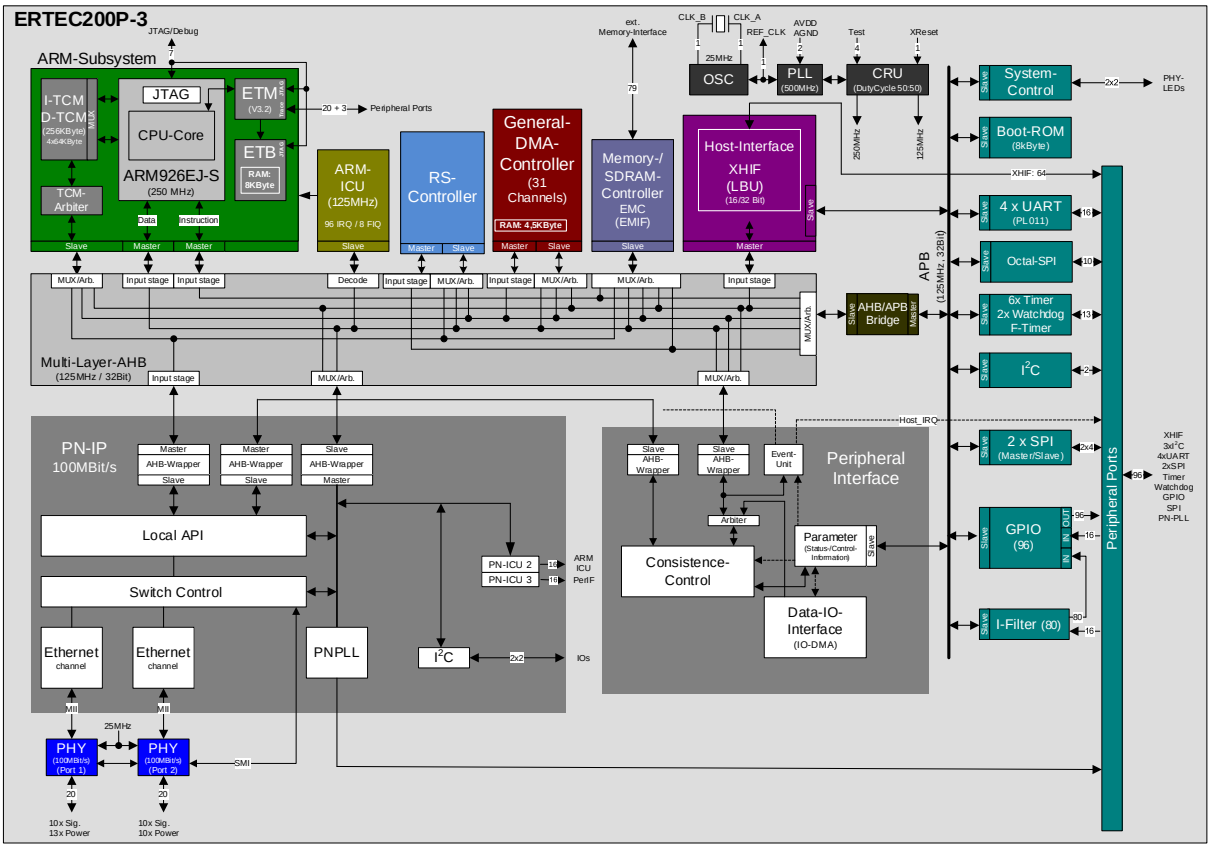

Figure 1-1: ERTEC 200P-3 Block Diagram

1.2 Key Functional Units

1.2.1 Processor Core Subsystem (ARM926)

- ARM926EJ-S Processor Core (revision r0p5)
- 8 KByte Boot ROM
- 256 KByte TCM
  - EDC with 1 Bit error correction and 2 Bit error detection with byte access
  - configurable as data (256-0 KByte) or instruction (0-256 KByte)-RAM
  - configuration-step: 64 KByte
- ARM Interrupt Controller
  - max. 96 interrupts
  - max. 8 fast interrupts
  - 8 software interrupt inputs and 86 hardware interrupt inputs
- Embedded Trace Macrocell (ETM9) for debugging
  - 8 address comparators
  - 4 address range comparators
  - 2 data comparators with filter functions
  - 4 trigger inputs (1 input ”EXTMEXTINO” available over alternate function)
  - 1 trigger output (available over alternate function)
  - 8 MMD regions to decode physical addresses
  - 3-stage sequenzer
  - 2 independent counters
  - FIFO size: 45 Byte
- JTAG block for debugging
- Memory Management Unit (MMU) with Translation Lookaside Buffers (TLBs)
- Separate Data and Instruction-Bus

1.2.2 Processor Bus Unit

- External Memory Controller (EMC)
  - SDRAM controller features:
    - 16 / 32 bit databus width
    - PC133 SDRAM-compatible (125 MHz synchron is used)
    - 1 Bank with max. 256 MByte SDRAM (32 Bit databus)
    - SDRAM support for following parts:
      - CAS-Latency: 2 or 3 clocks
      - Bank-address bits (1/2/4 internal banks), realized via the lowest two bits of the address bus MA(1:0)
      - 8 / 9 / 10 / 11 Bit column-address MA(13), MA(11:2)
      - max. 14 Bit row-address MA(15:2)
  - asynchronous controller features:
    - 8 / 16 / 32 Bit bus width (for each chip select programmable)
    - 4 chip selects
    - the timing for each chip select can be set individually
    - the response to ready signal can be set individually for each chip select
    - a maximum of 64 MByte address area for each chip select
- DMA Controller
  - 1 Channel
  - 32 Jobs
    - 20 can be started from hardware
    - 32 can be started from software
- Octal SPI via GPIO pins
- Two SPI
  - SPI1 via dedicated pins
  - SPI2 via GPIO pins

- UART interface via dedicated IO pins
- Timer Unit (Module TIMER_TOP)
  - reloadable Down-Counters
  - each timer is equipped with a multiplexer for trigger signals
- Interrupt Control Unit (Module ICU)
  - level or edge triggered operation
  - 96 interrupt request inputs
  - Interrupt priority is individually selectable for each request input
- Watchdog Unit
  - Watchdog interrupt generation via counter 0
  - Watchdog reset generation via counter 1
  - After initiating the watchdog timer, it will not stop counting unless the system is restarted.

1.2.3 PROFINET – IP

- 2 Ethernet-Ports
- 100MBit/s Ethernet-Port with integrated dual PHY
- Dynamic Frame Packing
- Fast Forwarding
- Short Preamble
- Dynamic Fragmentation
- IRT-Forwarding
- PNPLL
- Support for synchronization protocols (e.g., PTCP)

1.2.4 PerIF

- Supports consistence for IO data
  - 8 ARs
  - 1 Supervisor AR

2 IO Interface

2.1 Overview

Table 2-1: IO – pin count overview

Description	Voltage	BGA Balls
Functional signals		
Standard signals	3.3V	37
XHIF/GPIOs	3.3V/1.8V	96
EMC	1.8V	79
	Subtotal	**212**
Power-Supply		
VDD_CORE	1.1 V	8
AVDD_PLL	1.1 V	1
VDDD_PHY	1.1 V	0
VDDA_PHY	1.1 V	2
VDD33	3.3 V	3
VDD_OSPI	3.3/1.8 V	2
VDD_XHIF	3.3/1.8 V	3
VDD_EMC	1.8 V	3
VDDIOD_PHY	3.3 V	2
VDDIOA_PHY	3.3 V	4
AVDDHV_PLL	3.3 V	1
VSS	GND	105
VSSD_PHY	GND	0
VSSIOD_PHY	GND	0
VSSA_PHY	GND	2
VSSIOA_PHY	GND	2
	Subtotal	**138**
Oscillator		
XTAL1(in)	3.3V	1
XTAL2(in)	3.3V	1
REF_CLK, BYP_CLK	3.3V	2
	Subtotal	**4**
Test pins		
TMC1, TMC2 (inputs)	3.3V	2
TEST, TACT	3.3V	2
	Subtotal	**4**
	Total	**358**

2.2 Detailed Signal Description

The following notes belong to Table 2-2:

Active level low = Signal name X….;

*) Driver power of the EMC signals can be set on a group-specific basis (G1 – G9) in the SCRB_DRIVER_EMC register.

Values after reset for the different groups	@1.8 V:
- G1, G3, and G7	6 mA
- G2, G4, G5. G6, G8 and G9	8 mA

**) Driver power of GPIO(31-0) and XHIF interface GPIO(95-32); can be set on a signal-specific basis with the SCRB_DRIVEx_yGPIO SCRB.

Value after reset @3.3 V: 8 mA , @1.8V: 4 mA

***) Pull circuit for GPIO(31-0) and XHIF interface GPIO(95-32); can be set on a signal-specific basis with the SCRB_PULLx_yGPIO SCRB.

[1)] Peak current

[2)] Average current

[3)] merged to GND on substrate

[4)] merged to VDD_CORE on the substrate, therefore included in the VDD_CORE number

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Table 2-2: Detailed Signal Description

ERTEC 200P-3 ASIC																		
IO ring	ERTEC 200P (LFBGA358)	I/O direction	I/O current/mA	IO buffer	Buffer direction	Drive strength	Drive strength in STA (1p8v / 3p3v)	Pin load/pF (Synthese)	Pull-up/down	fout/MHz	Activity	Low Noise	Schmitt-Trigger	IO supply	Function	supply domain	supply domain name	ERTEC 200P Location
REF_CLK	1	out		LNBD12MDSTPS33	inout	8	8	50	-	25	1	-	-	3V3	Reference Clock MII (ext. PHY)		VDD33	A8
BYP_CLK	1	in		LNBD12MDSTPS33	inout	-	-	-	-	-	-	-	-	3V3	Clock for F-Timer		VDD33	E12
XRESET	1	in		LNBINST33	in	-	-	-	-	-	-	-	ST	3V3	PowerOn-Reset (lowaktiv)		VDD33	D9
XTAL1	1	in		LNAINHV	in	-	-	-	-	-	-	-	-	3V3	Oscillator in / Clk_in for oscillator bypass		VDD33	A9
XTAL2	1	out		LNOSCMD33O	out	2	2	20	-	25	1	-	-	3V3	Oscillator		VDD33	B9
TEST	1	in		LNBD12MDSTPS33	inout	-	-	-	DN	-	-	-	-	3V3	Test pin, has to be tied to GND in normal operation mode		VDD33	B10
TMC1	1	in		LNBD12MDSTPS33	inout	-	-	-	DN	-	-	-	-	3V3	Test Mode, has to be tied to GND in normal operation mode	●	VDD_XHIF	T6
TMC2	1	in		LNBD12MDSTPS33	inout	-	-	-	DN	-	-	-	-	3V3	Test Mode, has to be tied to GND in normal operation mode		VDD33	A7
TACT	1	in		LNBD12MDSTPS33	inout	-	-	-	DN	-	-	-	-	3V3	Test pin, has to be tied to GND in normal operation mode		VDD33	B8
TMS	1	in		LNBD12MDSTPS33	inout	-	-	-	UP	-	-	-	ST	3V3	JTAG: Test Mode Select		VDD33	E13
XTRST	1	in		LNBD12MDSTPS33	inout	-	-	-	DN	-	-	-	ST	3V3	JTAG: Reset		VDD33	B17
TCK	1	in		LNBD12MDSTPS33	inout	-	-	-	DN	-	-	-	ST	3V3	JTAG: Clock		VDD33	D16
RTCK	1	out		LNBD12MDSTPS33	inout	8	8	50	-	32	1	-	-	3V3	JTAG: Sync TCK		VDD33	B16
TDI	1	in		LNBD12MDSTPS33	inout	-	-	-	UP	-	-	-	ST	3V3	JTAG: Data In		VDD33	A16
TDO	1	out		LNBD12MDSTPS33	inout	8	8	50	-	32	0.5	-	-	3V3	JTAG: Data Out		VDD33	C16

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ERTEC 200P-3 ASIC																		
IO ring	ERTEC 200P (LFBGA358)	I/O direction	I/O current/mA	IO buffer	Buffer direction	Drive strength	Drive strength in STA (1p8v / 3p3v)	Pin load/pF (Synthese)	Pull-up/down	fout/MHz	Activity	Low Noise	Schmitt-Trigger	IO supply	Function	supply domain	supply domain name	ERTEC 200P Location
XSRST	1	bidi		LNBD12MDSTPS33	inout	8	8	50	UP	0.1	0.1	-	ST	3V3	System-Reset for Debugging		VDD33	C10
TAP_SEL	1	in		LNBD12MDSTPS33	inout	-	-	-	-	-	-	-	ST	3V3	TAP Select Signal: 0 = JTAG for debug 1 = JTAG for BS		VDD33	A17
CHAIN_CTRL	1	in		LNBD12MDSTPS33	inout	-	-	-	-	-	-	-	ST	3V3	Reserved		VDD33	E15
A0	1	bidi		ZLLNBD12MDSTPS33	inout	G2*)	6 / 8	20	-	42	0.1	-	-	1V8	EMC Address Bus Pin 0	●	VDD_EMC	N18
A1	1	bidi		ZLLNBD12MDSTPS33	inout	G2*)	6 / 8	20	-	42	0.1	-	-	1V8	EMC Address Bus Pin 1		VDD_EMC	R20
A2	1	bidi		ZLLNBD12MDSTPS33	inout	G2*)	6 / 8	20	DN	42	0.1	-	-	1V8	EMC Address Bus Pin 2 *DEV_HWK(5)*		VDD_EMC	T20
A3	1	bidi		ZLLNBD12MDSTPS33	inout	G2*)	6 / 8	20	DN	42	0.1	-	-	1V8	EMC Address Bus Pin 3 *DEV_HWK(6)*		VDD_EMC	R19
A4	1	bidi		ZLLNBD12MDSTPS33	inout	G2*)	6 / 8	20	DN	42	0.1	-	-	1V8	EMC Address Bus Pin 4 *DEV_HWK(7)*		VDD_EMC	P16
A5	1	bidi		ZLLNBD12MDSTPS33	inout	G2*)	6 / 8	20	UP	42	0.1	-	-	1V8	EMC Address Bus Pin 5		VDD_EMC	T18

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ERTEC 200P-3 ASIC																		
IO ring	ERTEC 200P (LFBGA358)	I/O direction	I/O current/mA	IO buffer	Buffer direction	Drive strength	Drive strength in STA (1p8v / 3p3v)	Pin load/pF (Synthese)	Pull-up/down	fout/MHz	Activity	Low Noise	Schmitt-Trigger	IO supply	Function	supply domain		supply domain name	ERTEC 200P Location
A6	1	bidi		ZLLNBD12MDSTPS33	inout	G2*)	6 / 8	20	UP	42	0.1	-	-	1V8	EMC Address Bus Pin 6			VDD_EMC	P17
A7	1	bidi		ZLLNBD12MDSTPS33	inout	G2*)	6 / 8	20	DN	42	0.1	-	-	1V8	EMC Address Bus Pin 7			VDD_EMC	P20
A8	1	bidi		ZLLNBD12MDSTPS33	inout	G2*)	6 / 8	20	DN	42	0.1	-	-	1V8	EMC Address Bus Pin 8 *DEV_HWK(0)*			VDD_EMC	P18
A9	1	bidi		ZLLNBD12MDSTPS33	inout	G2*)	6 / 8	20	DN	42	0.1	-	-	1V8	EMC Address Bus Pin 9 *DEV_HWK(1)*			VDD_EMC	P19
A10	1	bidi		ZLLNBD12MDSTPS33	inout	G2*)	6 / 8	20	DN	42	0.1	-	-	1V8	EMC Address Bus Pin 10 *DEV_HWK(2)*			VDD_EMC	N17
A11	1	bidi		ZLLNBD12MDSTPS33	inout	G2*)	6 / 8	20	DN	42	0.1	-	-	1V8	EMC Address Bus Pin 11 *DEV_HWK(3)*			VDD_EMC	M18
A12	1	bidi		ZLLNBD12MDSTPS33	inout	G2*)	6 / 8	20	DN	42	0.1	-	-	1V8	EMC Address Bus Pin 12 *DEV_HWK(4)*			VDD_EMC	M16
A13	1	bidi		ZLLNBD12MDSTPS33	inout	G2*)	6 / 8	20	UP	42	0.1	-	-	1V8	EMC Address Bus Pin 13			VDD_EMC	L20
A14	1	bidi		ZLLNBD12MDSTPS33	inout	G2*)	6 / 8	20	UP	42	0.1	-	-	1V8	EMC Address Bus Pin 14			VDD_EMC	K18
A15	1	bidi		LNBD12MDSTPS33	inout	G3*)	6 / 8	20	DN	42	0.1	-	-	1V8	EMC Address Bus Pin 15 *Boot(2)*			VDD_EMC	J18

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ERTEC 200P-3 ASIC																	
IO ring	ERTEC 200P (LFBGA358)	I/O direction	I/O current/mA	IO buffer	Buffer direction	Drive strength	Drive strength in STA (1p8v / 3p3v)	Pin load/pF (Synthese)	Pull-up/down	fout/MHz	Activity	Low Noise	Schmitt-Trigger	IO supply	Function	supply domain	supply domain name	ERTEC 200P Location
A16	1	bidi		LNBD12MDSTPS33	inout	G3*)	6 / 8	20	UP	42	0.1	-	-	1V8	EMC Address Bus Pin 16 *Boot(3)*		VDD_EMC	J20
A17	1	bidi		LNBD12MDSTPS33	inout	G3*)	6 / 8	20	UP	42	0.1	-	-	1V8	EMC Address Bus Pin 17 *Config(0)*		VDD_EMC	H20
A18	1	bidi		LNBD12MDSTPS33	inout	G3*)	6 / 8	20	UP	42	0.1	-	-	1V8	EMC Address Bus Pin 18 *Config(1)*		VDD_EMC	H18
A19	1	bidi		LNBD12MDSTPS33	inout	G3*)	6 / 8	20	DN	42	0.1	-	-	1V8	EMC Address Bus Pin 19 *Config(2)*		VDD_EMC	J16
A20	1	bidi		LNBD12MDSTPS33	inout	G3*)	6 / 8	20	UP	42	0.1	-	-	1V8	EMC Address Bus Pin 20 *Config(3)*		VDD_EMC	H19
A21	1	bidi		LNBD12MDSTPS33	inout	G3*)	6 / 8	20	DN	42	0.1	-	-	1V8	EMC Address Bus Pin 21 *Config(4)*		VDD_EMC	G19
A22	1	bidi		LNBD12MDSTPS33	inout	G3*)	6 / 8	20	DN	42	0.1	-	-	1V8	EMC Address Bus Pin 22 *Config(5)*		VDD_EMC	G20
A23	1	bidi		LNBD12MDSTPS33	inout	G3*)	6 / 8	20	UP	42	0.1	-	-	1V8	EMC Address Bus Pin 23 *Config(6)*		VDD_EMC	H17
D0	1	bidi		ZLLNBD12MDSTPS33	inout	G4*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 0		VDD_EMC	A18
D1	1	bidi		ZLLNBD12MDSTPS33	inout	G4*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 1		VDD_EMC	B20
D2	1	bidi		ZLLNBD12MDSTPS33	inout	G4*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 2		VDD_EMC	C19

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ERTEC 200P-3 ASIC																		
IO ring	ERTEC 200P (LFBGA358)	I/O direction	I/O current/mA	IO buffer	Buffer direction	Drive strength	Drive strength in STA (1p8v / 3p3v)	Pin load/pF (Synthese)	Pull-up/down	fout/MHz	Activity	Low Noise	Schmitt-Trigger	IO supply	Function	supply domain		supply domain name	ERTEC 200P Location
D3	1	bidi		ZLLNBD12MDSTPS33	inout	G4*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 3			VDD_EMC	C18
D4	1	bidi		ZLLNBD12MDSTPS33	inout	G4*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 4			VDD_EMC	B19
D5	1	bidi		ZLLNBD12MDSTPS33	inout	G4*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 5			VDD_EMC	G16
D6	1	bidi		ZLLNBD12MDSTPS33	inout	G4*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 6			VDD_EMC	E17
D7	1	bidi		ZLLNBD12MDSTPS33	inout	G4*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 7			VDD_EMC	D20
D8	1	bidi		ZLLNBD12MDSTPS33	inout	G4*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 8			VDD_EMC	F18
D9	1	bidi		ZLLNBD12MDSTPS33	inout	G4*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 9			VDD_EMC	D19
D10	1	bidi		ZLLNBD12MDSTPS33	inout	G4*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 10			VDD_EMC	E20
D11	1	bidi		ZLLNBD12MDSTPS33	inout	G4*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 11			VDD_EMC	D17
D12	1	bidi		ZLLNBD12MDSTPS33	inout	G4*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 12			VDD_EMC	D18
D13	1	bidi		ZLLNBD12MDSTPS33	inout	G4*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 13			VDD_EMC	A19
D14	1	bidi		ZLLNBD12MDSTPS33	inout	G4*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 14			VDD_EMC	C20
D15	1	bidi		ZLLNBD12MDSTPS33	inout	G4*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 15			VDD_EMC	B18
D16	1	bidi		ZLLNBD12MDSTPS33	inout	G5*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 16			VDD_EMC	R17
D17	1	bidi		ZLLNBD12MDSTPS33	inout	G5*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 17			VDD_EMC	U17
D18	1	bidi		ZLLNBD12MDSTPS33	inout	G5*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 18			VDD_EMC	V20

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ERTEC 200P-3 ASIC																		
IO ring	ERTEC 200P (LFBGA358)	I/O direction	I/O current/mA	IO buffer	Buffer direction	Drive strength	Drive strength in STA (1p8v / 3p3v)	Pin load/pF (Synthese)	Pull-up/down	fout/MHz	Activity	Low Noise	Schmitt-Trigger	IO supply	Function	supply domain		supply domain name	ERTEC 200P Location
D19	1	bidi		ZLLNBD12MDSTPS33	inout	G5*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 19			VDD_EMC	V17
D20	1	bidi		ZLLNBD12MDSTPS33	inout	G5*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 20			VDD_EMC	W20
D21	1	bidi		ZLLNBD12MDSTPS33	inout	G5*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 21			VDD_EMC	V16
D22	1	bidi		ZLLNBD12MDSTPS33	inout	G5*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 22			VDD_EMC	Y19
D23	1	bidi		ZLLNBD12MDSTPS33	inout	G5*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 23			VDD_EMC	Y18
D24	1	bidi		ZLLNBD12MDSTPS33	inout	G5*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 24			VDD_EMC	Y17
D25	1	bidi		ZLLNBD12MDSTPS33	inout	G5*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 25			VDD_EMC	U16
D26	1	bidi		ZLLNBD12MDSTPS33	inout	G5*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 26			VDD_EMC	W17
D27	1	bidi		ZLLNBD12MDSTPS33	inout	G5*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 27			VDD_EMC	V18
D28	1	bidi		ZLLNBD12MDSTPS33	inout	G5*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 28			VDD_EMC	W18
D29	1	bidi		ZLLNBD12MDSTPS33	inout	G5*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 29			VDD_EMC	T17
D30	1	bidi		ZLLNBD12MDSTPS33	inout	G5*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 30			VDD_EMC	W19
D31	1	bidi		ZLLNBD12MDSTPS33	inout	G5*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Data Bus Pin 31			VDD_EMC	V19
XBE0_DQM0	1	bidi		ZLLNBD12MDSTPS33	inout	G4*)	6 / 12	20	-	42	0.1	-	-	1V8	EMC Byte 0 Enable			VDD_EMC	F19
XBE1_DQM1	1	bidi		ZLLNBD12MDSTPS33	inout	G4*)	6 / 12	20	-	42	0.1	-	-	1V8	EMC Byte 1 Enable			VDD_EMC	F20
XBE2_DQM2	1	bidi		ZLLNBD12MDSTPS33	inout	G5*)	6 / 12	20	-	42	0.1	-	-	1V8	EMC Byte 2 Enable			VDD_EMC	T19

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ERTEC 200P-3 ASIC																		
IO ring	ERTEC 200P (LFBGA358)	I/O direction	I/O current/mA	IO buffer	Buffer direction	Drive strength	Drive strength in STA (1p8v / 3p3v)	Pin load/pF (Synthese)	Pull-up/down	fout/MHz	Activity	Low Noise	Schmitt-Trigger	IO supply	Function	supply domain		supply domain name	ERTEC 200P Location
XBE3_DQM3	1	bidi		ZLLNBD12MDSTPS33	inout	G5*)	6 / 12	20	-	42	0.1	-	-	1V8	EMC Byte 3 Enable			VDD_EMC	U18
XCS_PER0	1	bidi		LNBD12MDSTPS33	inout	G7*)	6 / 12	20	-	1	1	-	-	1V8	EMC Bank 0 Chip Select			VDD_EMC	G18
XCS_PER1	1	bidi		LNBD12MDSTPS33	inout	G7*)	6 / 12	20	-	1	1	-	-	1V8	EMC Bank 1 Chip Select			VDD_EMC	G17
XCS_PER2	1	bidi		LNBD12MDSTPS33	inout	G7*)	6 / 12	20	-	1	1	-	-	1V8	EMC Bank 2 Chip Select			VDD_EMC	U20
XCS_PER3	1	bidi		LNBD12MDSTPS33	inout	G7*)	6 / 12	20	-	1	1	-	-	1V8	EMC Bank 3 Chip Select			VDD_EMC	R18
XWR	1	bidi		ZLLNBD12MDSTPS33	inout	G6*)	6 / 12	20	-	42	0.1	-	-	1V8	EMC Write Signal			VDD_EMC	J17
XRD	1	bidi		ZLLNBD12MDSTPS33	inout	G6*)	6 / 12	20	-	42	0.1	-	-	1V8	EMC Read Signal			VDD_EMC	K16
XRDY_PER	1	bidi		ZLLNBD12MDSTPS33	inout	G4*)	6 / 12	20	UP	62.5	0.16	-	-	1V8	EMC Ready Signal			VDD_EMC	M17
DTXR	1	bidi		LNBD12MDSTPS33	inout	G1*)	6 / 12	20	DN	42	0.1	-	-	1V8	EMC Direction for ext. Driver *Boot(0)*			VDD_EMC	E18
XOE_DRIVER	1	bidi		LNBD12MDSTPS33	inout	G1*)	6 / 12	20	UP	1	1	-	-	1V8	EMC Enable for ext. Driver *Boot(1)*			VDD_EMC	F17
CLK_O_SDRAM0	1	out		ZLLNBD12MDSTPS33	inout	G8*)	6 / 8	20	-	125	1	-	-	1V8	Feedback clock output			VDD_EMC	N20
CLK_O_SDRAM1	1	out		ZLLNBD12MDSTPS33	inout	G8*)	6 / 8	20	-	125	1	-	-	1V8	clock for the SDRAM device			VDD_EMC	L17
CLK_O_SDRAM2	1	out		ZLLNBD12MDSTPS33	inout	G8*)	6 / 8	20	-	125	1	-	-	1V8	clock for the SDRAM device			VDD_EMC	L18
CLK_I_SDRAM	1	in		LNBD12MDSTPS33	inout	-	-	-	-	-	-	-	-	1V8	Feedback clock for synchronization of read data. Must be connected, even if SDRAM is not used!			VDD_EMC	N16

ERTEC 200P-3 ASIC																		
IO ring	ERTEC 200P (LFBGA358)	I/O direction	I/O current/mA	IO buffer	Buffer direction	Drive strength	Drive strength in STA (1p8v / 3p3v)	Pin load/pF (Synthese)	Pull-up/down	fout/MHz	Activity	Low Noise	Schmitt-Trigger	IO supply	Function	supply domain	supply domain name	ERTEC 200P Location
XCS_SDRAM	1	bidi		ZLLNBD12MDSTPS33	inout	G9*)	6 / 12	20	-	5	0.1	-	-	1V8	Chip select for SDRAM		VDD_EMC	M20
XRAS_SDRAM	1	out		ZLLNBD12MDSTPS33	inout	G9*)	6 / 12	20	-	5	0.1	-	-	1V8	Row address strobe		VDD_EMC	M19
XCAS_SDRAM	1	bidi		ZLLNBD12MDSTPS33	inout	G9*)	6 / 12	20	-	5	0.1	-	-	1V8	Column address strobe		VDD_EMC	L19
XWE_SDRAM	1	out		ZLLNBD12MDSTPS33	inout	G9*)	6 / 12	20	-	5	0.1	-	-	1V8	Write enable for SDRAM		VDD_EMC	K20
XAV_BF	1	in		LNBD12MDSTPS33	inout	-	-	-	UP	-	-	-	-	1V8	Address Valid BurstFlash **--> not used** *Boot(4)*		VDD_EMC	K19
XRDY_BF	1	in		LNBD12MDSTPS33	inout	-	-	-	UP	-	-	-	-	1V8	Ready BurstFlash **--> not used** *EXT_DRIVER_DISABLE_CS0*	•	VDD_EMC	K17
P1RXN	1	inout	100[1)]		-	-	-	-	-	-	-	-	-	3V3	Port1 differential receive input	•	VDDIOA_PHY	T3
P1RXP	1	inout	100[1)]		-	-	-	-	-	-	-	-	-	3V3			VDDIOA_PHY	T4
P1TXN	1	inout	100[1)]		-	-	-	-	-	125	0.5	-	-	3V3	Port1 differential transmit output		VDDIOA_PHY	R1
P1TXP	1	inout	100[1)]		-	-	-	-	-	125	0.5	-	-	3V3			VDDIOA_PHY	R2
P1RDXP	1	in			in	-	-	-	-	-	-	-	-	3V3	Port1 FX differential receive input (PECL)		VDDIOA_PHY	U2
P1RDXN	1	in			in	-	-	-	-	-	-	-	-	3V3			VDDIOA_PHY	U1
P1TDXP	1	out	55[1)]		out	-	-	-	-	125	0.5	-	-	3V3	Port1 FX differential transmit output (PECL)		VDDIOA_PHY	W2
P1TDXN	1	out	55[1)]		out	-	-	-	-	125	0.5	-	-	3V3			VDDIOA_PHY	W1
P1SDXP	1	in			in	-	-	-	-	-	-	-	-	3V3	Port1 FX SD input (PECL)		VDDIOA_PHY	V4

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ERTEC 200P-3 ASIC																		
IO ring	ERTEC 200P (LFBGA358)	I/O direction	I/O current/mA	IO buffer	Buffer direction	Drive strength	Drive strength in STA (1p8v / 3p3v)	Pin load/pF (Synthese)	Pull-up/down	fout/MHz	Activity	Low Noise	Schmitt-Trigger	IO supply	Function	supply domain	supply domain name	ERTEC 200P Location
P1SDXN	1	in			in	-	-	-	-	-	-	-	-	3V3			VDDIOA_PHY	V3
P2RXN	1	inout	100[1)]		in	-	-	-	-	-	-	-	-	3V3	Port2 differential receive input		VDDIOA_PHY	E3
P2RXP	1	inout	100[1)]		in	-	-	-	-	-	-	-	-	3V3			VDDIOA_PHY	E4
P2TXN	1	inout	100[1)]		-	-	-	-	-	125	0.5	-	-	3V3	Port2 differential transmit output		VDDIOA_PHY	F1
P2TXP	1	inout	100[1)]		-	-	-	-	-	125	0.5	-	-	3V3			VDDIOA_PHY	F2
P2RDXP	1	in			in	-	-	-	-	-	-	-	-	3V3	Port2 FX differential receive input (PECL)		VDDIOA_PHY	D2
P2RDXN	1	in			in	-	-	-	-	-	-	-	-	3V3			VDDIOA_PHY	D1
P2TDXP	1	out	55[1)]		-	-	-	-	-	125	0.5	-	-	3V3	Port2 FX differential transmit output (PECL)		VDDIOA_PHY	B2
P2TDXN	1	out	55[1)]		-	-	-	-	-	125	0.5	-	-	3V3			VDDIOA_PHY	B1
P2SDXP	1	in			in	-	-	-	-	-	-	-	-	3V3	Port2 FX SD input (PECL)		VDDIOA_PHY	C4
P2SDXN	1	in			in	-	-	-	-	-	-	-	-	3V3		•	VDDIOA_PHY	C3
P1FXEN	1	out			out	12	12	20	-	0	-	-	-	3V3	Port1 FX enable	•	VDDIOD_PHY	P3
P2FXEN	1	out			out	12	12	20	-	0	-	-	-	3V3	Port2 FX enable	•	VDDIOD_PHY	G3
L_PHY_1	1	out		LNBD12MDSTPS33	inout	8	8	20	-	0.1	0.1	-	-	3V3	Link LED PHY Port 1		VDD33	D5
A_PHY_1	1	out		LNBD12MDSTPS33	inout	8	8	20	-	0.1	0.1	-	-	3V3	Activity LED PHY Port 1		VDD33	A3
L_PHY_2	1	out		LNBD12MDSTPS33	inout	8	8	20	-	0.1	0.1	-	-	3V3	Link LED PHY Port 2		VDD33	E6

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ERTEC 200P-3 ASIC																	
IO ring	ERTEC 200P (LFBGA358)	I/O direction	I/O current/mA	IO buffer	Buffer direction	Drive strength	Drive strength in STA (1p8v / 3p3v)	Pin load/pF (Synthese)	Pull-up/down	fout/MHz	Activity	Low Noise	Schmitt-Trigger	IO supply	Function	supply domain	supply domain name	ERTEC 200P Location
A_PHY_2	1	out		LNBD12MDSTPS33	inout	8	8	20	-	0.1	0.1	-	-	3V3	Activity LED PHY Port 2		VDD33	A4
GPIO0_INT	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 0 (interrupt capable) --- *I-Filter: IN_Delay_0*		VDD33	C15
GPIO1_INT	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 1 (interrupt capable) --- *I-Filter: IN_Delay_1*		VDD33	D15
GPIO2_INT	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 2 (interrupt capable) --- *I-Filter: IN_Delay_2*		VDD33	B15
GPIO3_INT	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 3 (interrupt capable) --- *I-Filter: IN_Delay_3*		VDD33	E14
GPIO4_INT	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 4 (interrupt capable) --- *I-Filter: IN_Delay_4*		VDD33	D14
GPIO5_INT	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 5 (interrupt capable) --- *I-Filter: IN_Delay_5*		VDD33	A15
GPIO6_INT	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 6 (interrupt capable) --- *I-Filter: IN_Delay_6*		VDD33	B14
GPIO7_INT	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 7 (interrupt capable) --- *I-Filter: IN_Delay_7*		VDD33	A14
GPIO8_INT	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 8 (interrupt capable) --- *I-Filter: IN_Delay_8*		VDD33	E11
GPIO9_INT	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 9 (interrupt capable) --- *I-Filter: IN_Delay_9*		VDD33	D11
GPIO10_INT	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 10 (interrupt capable) --- *I-Filter: IN_Delay_10*		VDD33	B11

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ERTEC 200P-3 ASIC																	
IO ring	ERTEC 200P (LFBGA358)	I/O direction	I/O current/mA	IO buffer	Buffer direction	Drive strength	Drive strength in STA (1p8v / 3p3v)	Pin load/pF (Synthese)	Pull-up/down	fout/MHz	Activity	Low Noise	Schmitt-Trigger	IO supply	Function	supply domain	supply domain name	ERTEC 200P Location
GPIO11_INT	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 11 (interrupt capable) --- *I-Filter: IN_Delay_11*		VDD33	A12
GPIO12_INT	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 12 (interrupt capable) --- *I-Filter: IN_Delay_12*		VDD33	A11
GPIO13_INT	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 13 (interrupt capable) --- *I-Filter: IN_Delay_13*		VDD33	D12
GPIO14_INT	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 14 (interrupt capable) --- *I-Filter: IN_Delay_14*		VDD33	B12
GPIO15_INT	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 15 (interrupt capable) --- *I-Filter: IN_Delay_15*		VDD33	B13
GPIO16	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 16		VDD33	D13
GPIO17	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 17		VDD33	C13
GPIO18	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 18		VDD33	A13
GPIO19	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 19		VDD33	C12
GPIO20	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 20		VDD33	C7
GPIO21	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 21		VDD33	B6
GPIO22	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 22		VDD33	D6
GPIO23	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 23		VDD33	B5

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ERTEC 200P-3 ASIC																		
IO ring	ERTEC 200P (LFBGA358)	I/O direction	I/O current/mA	IO buffer	Buffer direction	Drive strength	Drive strength in STA (1p8v / 3p3v)	Pin load/pF (Synthese)	Pull-up/down	fout/MHz	Activity	Low Noise	Schmitt-Trigger	IO supply	Function	supply domain	supply domain name	ERTEC 200P Location
GPIO24	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 24		VDD33	A6
GPIO25	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 25		VDD33	A5
GPIO26	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 26		VDD33	C8
GPIO27	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 27		VDD33	C6
GPIO28	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 28		VDD33	D8
GPIO29	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 29		VDD33	B7
GPIO30	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 30		VDD33	D7
GPIO31	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.001	-	ST	3V3	GPIO 31		VDD33	E7
XHIF_A1	1	bidi		LNBD12MDSTPS33C2	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 1 / GPIO 32 --- *I-Filter: IN_Delay_16*	•	VDD_OSPI	W10
XHIF_A2	1	bidi		LNBD12MDSTPS33C2	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 2 / GPIO 33 --- *I-Filter: IN_Delay_17*		VDD_OSPI	W11
XHIF_A3	1	bidi		LNBD12MDSTPS33C2	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 3 / GPIO 34 --- *I-Filter: IN_Delay_18*		VDD_OSPI	W9
XHIF_A4	1	bidi		LNBD12MDSTPS33C2	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 4 / GPIO 35 --- *I-Filter: IN_Delay_19*		VDD_OSPI	V11
XHIF_A5	1	bidi		LNBD12MDSTPS33C2	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 5 / GPIO 36 --- *I-Filter: IN_Delay_20*		VDD_OSPI	Y10
XHIF_A6	1	bidi		LNBD12MDSTPS33C2	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 6 / GPIO 37 --- *I-Filter: IN_Delay_21*		VDD_OSPI	Y8
XHIF_A7	1	bidi		LNBD12MDSTPS33C2	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 7 / GPIO 38 --- *I-Filter: IN_Delay_22*		VDD_OSPI	Y9
XHIF_A8	1	bidi		LNBD12MDSTPS33C2	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 8 / GPIO 39 ---*I-Filter: IN_Delay_23*		VDD_OSPI	Y11

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ERTEC 200P-3 ASIC																		
IO ring	ERTEC 200P (LFBGA358)	I/O direction	I/O current/mA	IO buffer	Buffer direction	Drive strength	Drive strength in STA (1p8v / 3p3v)	Pin load/pF (Synthese)	Pull-up/down	fout/MHz	Activity	Low Noise	Schmitt-Trigger	IO supply	Function	supply domain	supply domain name	ERTEC 200P Location
XHIF_A9	1	bidi		LNBD12MDSTPS33C2	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 9 / GPIO 40 --- *I-Filter: IN_Delay_24*		VDD_OSPI	W8
XHIF_A10	1	bidi		LNBD12MDSTPS33C2	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 10 / GPIO 41 --- *I-Filter: IN_Delay_25*		VDD_OSPI	W7
XHIF_A11	1	bidi		LNBD12MDSTPS33C2	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 11 / GPIO 42 --- *I-Filter: IN_Delay_26*	•	VDD_OSPI	Y7
XHIF_A12	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 12 / GPIO 43 --- *I-Filter: IN_Delay_27*	•	VDD_XHIF	V6
XHIF_A13	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 13 / GPIO 44 --- *I-Filter: IN_Delay_28*		VDD_XHIF	Y6
XHIF_A14	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 14 / GPIO 45 --- *I-Filter: IN_Delay_29*		VDD_XHIF	W13
XHIF_A15	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 15 / GPIO 46 --- *I-Filter: IN_Delay_30*		VDD_XHIF	U7
XHIF_A16	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 16 / GPIO 47 --- *I-Filter: IN_Delay_31*		VDD_XHIF	U9
XHIF_A17	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 17 / GPIO 48 --- *I-Filter: IN_Delay_32*		VDD_XHIF	V8
XHIF_A18	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 18 / GPIO 49 --- *I-Filter: IN_Delay_33*		VDD_XHIF	T8
XHIF_A19	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 19 / GPIO 50 --- *I-Filter: IN_Delay_34*		VDD_XHIF	T7
XHIF_SEG_2	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 22 / GPIO 51 --- I-Filter: IN_Delay_37		VDD_XHIF	W6
XHIF_SEG_0	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 20 / GPIO 52 --- I-Filter: IN_Delay_35		VDD_XHIF	Y3
XHIF_SEG_1	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Address Bus Pin 21 / GPIO 53 --- I-Filter: IN_Delay_36		VDD_XHIF	W5

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ERTEC 200P-3 ASIC																		
IO ring	ERTEC 200P (LFBGA358)	I/O direction	I/O current/mA	IO buffer	Buffer direction	Drive strength	Drive strength in STA (1p8v / 3p3v)	Pin load/pF (Synthese)	Pull-up/down	fout/MHz	Activity	Low Noise	Schmitt-Trigger	IO supply	Function	supply domain		supply domain name	ERTEC 200P Location
XHIF_XRDY	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.100	-	ST	1V8/3V3	XHIF Ready Signal, polarity adjustable / GPIO 54 *--- I-Filter: IN_Delay_46*			VDD_XHIF	J1
XHIF_XIRQ	1	bidi		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.100	-	ST	1V8/3V3	XHIF Interrupt Output / GPIO 55 *--- I-Filter: IN_Delay_47*			VDD_XHIF	N4
XHIF_XWR	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Write Signal, lowactive / GPIO 56 *--- I-Filter: IN_Delay_45*			VDD_XHIF	U5
XHIF_XRD	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Read Signal, lowactive / GPIO 57 *--- I-Filter: IN_Delay_44*			VDD_XHIF	Y4
XHIF_XCS_R_A20	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Chip Select for Page Config. Registers / GPIO 58 *--- I-Filter: IN_Delay_43*			VDD_XHIF	Y5
XHIF_XCS_M	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Chip Select for AHB access / GPIO 59 *--- I-Filter: IN_Delay_42*			VDD_XHIF	V7
XHIF_XBE0	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Byte 0 Enable, lowactive / GPIO 60 *--- I-Filter: IN_Delay_38*			VDD_XHIF	N3
XHIF_XBE1	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Byte 1 Enable, lowactive / GPIO 61 *--- I-Filter: IN_Delay_39*			VDD_XHIF	N2
XHIF_XBE2	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Byte 2 Enable, lowactive / GPIO 62 *--- I-Filter: IN_Delay_40*			VDD_XHIF	Y12
XHIF_XBE3	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	-	-	ST	1V8/3V3	XHIF Byte 3 Enable, lowactive / GPIO 63 *--- I-Filter: IN_Delay_41*			VDD_XHIF	T11

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ERTEC 200P-3 ASIC																		
IO ring	ERTEC 200P (LFBGA358)	I/O direction	I/O current/mA	IO buffer	Buffer direction	Drive strength	Drive strength in STA (1p8v / 3p3v)	Pin load/pF (Synthese)	Pull-up/down	fout/MHz	Activity	Low Noise	Schmitt-Trigger	IO supply	Function	supply domain		supply domain name	ERTEC 200P Location
XHIF_D0	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 0 / GPIO 64 - *-- I-Filter: IN_Delay_48*			VDD_XHIF	M3
XHIF_D1	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 1 / GPIO 65 - *-- I-Filter: IN_Delay_49*			VDD_XHIF	K3
XHIF_D2	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 2 / GPIO 66 - *-- I-Filter: IN_Delay_50*			VDD_XHIF	H1
XHIF_D3	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 3 / GPIO 67 - *-- I-Filter: IN_Delay_51*			VDD_XHIF	N1
XHIF_D4	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 4 / GPIO 68 - *-- I-Filter: IN_Delay_52*			VDD_XHIF	M1
XHIF_D5	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 5 / GPIO 69 - *-- I-Filter: IN_Delay_53*			VDD_XHIF	K1
XHIF_D6	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 6 / GPIO 70 - *-- I-Filter: IN_Delay_54*			VDD_XHIF	J4
XHIF_D7	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 7 / GPIO 71 - *-- I-Filter: IN_Delay_55*			VDD_XHIF	L2
XHIF_D8	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 8 / GPIO 72 - *-- I-Filter: IN_Delay_56*			VDD_XHIF	L1
XHIF_D9	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 9 / GPIO 73 - *-- I-Filter: IN_Delay_57*			VDD_XHIF	K4
XHIF_D10	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 10 / GPIO 74 *--- I-Filter: IN_Delay_58*			VDD_XHIF	J2
XHIF_D11	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 11 / GPIO 75 *--- I-Filter: IN_Delay_59*			VDD_XHIF	L4
XHIF_D12	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 12 / GPIO 76 *--- I-Filter: IN_Delay_60*			VDD_XHIF	M4
XHIF_D13	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 13 / GPIO 77 *--- I-Filter: IN_Delay_61*			VDD_XHIF	J3
XHIF_D14	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 14 / GPIO 78 *--- I-Filter: IN_Delay_62*			VDD_XHIF	L3

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ERTEC 200P-3 ASIC																		
IO ring	ERTEC 200P (LFBGA358)	I/O direction	I/O current/mA	IO buffer	Buffer direction	Drive strength	Drive strength in STA (1p8v / 3p3v)	Pin load/pF (Synthese)	Pull-up/down	fout/MHz	Activity	Low Noise	Schmitt-Trigger	IO supply	Function	supply domain		supply domain name	ERTEC 200P Location
XHIF_D15	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 15 / GPIO 79 *--- I-Filter: IN_Delay_63*			VDD_XHIF	H2
XHIF_D16	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 16 / GPIO 80 *--- I-Filter: IN_Delay_64*			VDD_XHIF	W15
XHIF_D17	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 17 / GPIO 81 *--- I-Filter: IN_Delay_65*			VDD_XHIF	U15
XHIF_D18	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 18 / GPIO 82 *--- I-Filter: IN_Delay_66*			VDD_XHIF	W14
XHIF_D19	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 19 / GPIO 83 *--- I-Filter: IN_Delay_67*			VDD_XHIF	Y16
XHIF_D20	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 20 / GPIO 84 *--- I-Filter: IN_Delay_68*			VDD_XHIF	U14
XHIF_D21	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 21 / GPIO 85 *--- I-Filter: IN_Delay_69*			VDD_XHIF	U11
XHIF_D22	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 22 / GPIO 86 *--- I-Filter: IN_Delay_70*			VDD_XHIF	Y14
XHIF_D23	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 23 / GPIO 87 *--- I-Filter: IN_Delay_71*			VDD_XHIF	Y15
XHIF_D24	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 24 / GPIO 88 *--- I-Filter: IN_Delay_72*			VDD_XHIF	T13
XHIF_D25	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 25 / GPIO 89 *--- I-Filter: IN_Delay_73*			VDD_XHIF	V15
XHIF_D26	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 26 / GPIO 90 *--- I-Filter: IN_Delay_74*			VDD_XHIF	Y13
XHIF_D27	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 27 / GPIO 91 *--- I-Filter: IN_Delay_75*			VDD_XHIF	V13
XHIF_D28	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 28 / GPIO 92 *--- I-Filter: IN_Delay_76*			VDD_XHIF	U12
XHIF_D29	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 29 / GPIO 93 *--- I-Filter: IN_Delay_77*			VDD_XHIF	U13

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ERTEC 200P-3 ASIC																		
IO ring	ERTEC 200P (LFBGA358)	I/O direction	I/O current/mA	IO buffer	Buffer direction	Drive strength	Drive strength in STA (1p8v / 3p3v)	Pin load/pF (Synthese)	Pull-up/down	fout/MHz	Activity	Low Noise	Schmitt-Trigger	IO supply	Function	supply domain	supply domain name	ERTEC 200P Location
XHIF_D30	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 30 / GPIO 94 *--- I-Filter: IN_Delay_78*		VDD_XHIF	T12
XHIF_D31	1	bidi[4)]		LNBD12MDSTPS33	inout	**)	8	20	***)	125	0.050	-	ST	1V8/3V3	XHIF Data Bus Pin 31 / GPIO 95 *--- I-Filter: IN_Delay_79*	●	VDD_XHIF	W12
VQPS	1	in			in	-	-	-	-	-	-	-	-	2V5	Reserved tied to GND	●		J5
VDD_CORE	8														1.1 V (Core Supply)			
AVDD_PLL	1														1.1V analog voltage supply for 500 MHz PLL and for 1600 MHz PLL, requires external filtering			
VDDD_PHY	-[4)]		180[2)]												1.1V (PHY Digital Core Supply)			
VDDA_PHY	2		20[2)]												1.1V (PHY Analog Core Supply)			
VDD33	3														3.3 V (IO Supply)			
VDD_OSPI	2														1.8 V / 3.3V (IO Supply)			
VDD_XHIF	3														3.3V / 1.8V (HostIF IO Supply)			
VDD_EMC	3														1.8V (EMC IO Supply)			
VDDIOD_PHY	2		30[2)]												3.3V (PHY Digital I/O Supply)			

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ERTEC 200P-3 ASIC																	
IO ring	ERTEC 200P (LFBGA358)	I/O direction	I/O current/mA	IO buffer	Buffer direction	Drive strength	Drive strength in STA (1p8v / 3p3v)	Pin load/pF (Synthese)	Pull-up/down	fout/MHz	Activity	Low Noise	Schmitt-Trigger	IO supply	Function	supply domain	supply domain name	ERTEC 200P Location
VDDIOA_PHY	4		130[2)]	3.3V (PHY Analog I/O Supply)														
AVDDHV_PLL	1			3.3V analog voltage supply for 500 MHz PLL and for 1600 MHz PLL														
VSS	105			Ground (includes AGND for PLLs and LVDS)														
VSSD_PHY	- [3)]		180[2)]	PHY digital core ground														
VSSIOD_PHY	- [3)]		30[2)]	PHY digital I/O ground														
VSSA_PHY	2		20[2)]	PHY analog core ground														
VSSIOA_PHY	2		250[2)]	PHY analog I/O ground														

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2.2.1 Strapping Pins

While XRESET is active, the input values of the following pins are latched in:

Table 2-3: Strapping Pins

Package Ball Name	Strapping Information	Remark
A_7	Reserved == 0	Values saved in SETUP_REG of SCRB2
A_8	DEV_HWK(0)	
A_9	DEV_HWK(1)	
A_10	DEV_HWK(2)	
A_11	DEV_HWK(3)	
A_12	DEV_HWK(4)	
A_2	DEV_HWK(5)	
A_3	DEV_HWK(6)	
A_4	DEV_HWK(7)	
A_17	Config(0)	Values saved in CONFIG_REG of SCRB1
A_18	Config(1)	
A_19	Config(2)	
A_20	Config(3)	
A_21	Config(4)	
A_22	Config(5)	
A_23	Config(6)	
DTXR	Boot(0)	Values saved in BOOT_REG of SCRB1
XOE_DRIVER	Boot(1)	
A_15	Boot(2)	
A_16	Boot(3)	
XAV_BF	Boot(4)	
XRDY_BF	*EXT_DRIVER_DISABLE_CS0*	Values saved in EXT_DRIVER_EN of SCRB1

Note

After XRESET is released, the values are stored. The values must stay stable for 500 ns after XRESET has been released. This is a difference compared to ERTEC 200P-2 (there only 120 ns are required).

For the configuration of Boot and Config modes external resistors must be used. The internal ones are not sufficient.

2.3 IO Timing

General rule:

For IO signals whose timing response is not detailed in the following chapters, there are no specific IO timing requirements. These signals therefore have default constraining, i.e. the selected constraining achieves IO timing closure without relaxing IO timing too much.

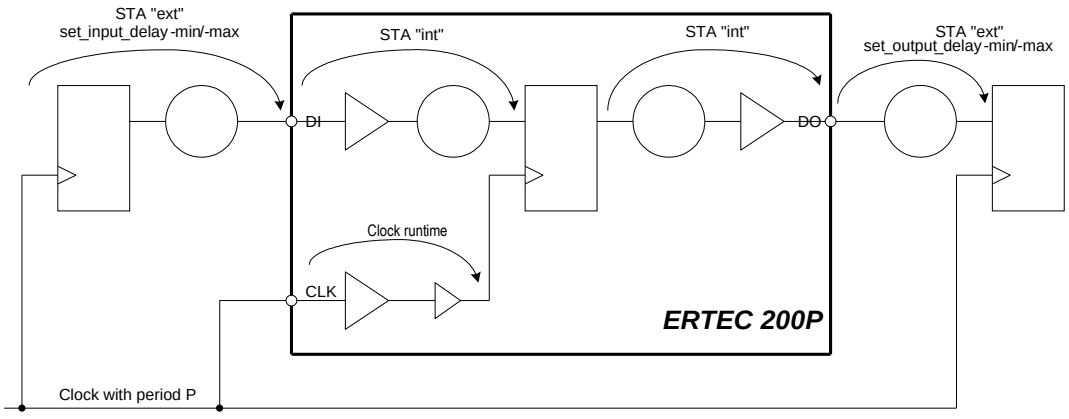

Figure 2-1: Definition of time reference

The constraint specifications correspond to the data sheet values as follows:

Input delay –min X	Input signal hold time => X
Input delay –max X	Input signal setup time => Period - X
Output delay –min X	Output signal hold time => X
Output delay –max X	Clock-to-output time of output signal => Period - X

2.3.1 EMC Timing

Note:

To achieve the timing below, configure EXTENDED_CONFIG.SODM = '0' (default value). EXTENDED_CONFIG.SODM = '1' is not permitted.

2.3.1.1 SRAM Timing

The use of XRDY_PER is optional and can be enabled with ASYNC_BANKx.EW. Wait states can be inserted if XRDY_PER is used.

For the asynchronous SRAM interface an **"active interface"** is selectable. Active interface means that at the end of a transfer the data bus is actively driven high for one AHB clock cycle. This is necessary, in combination with the use of internal Pull-up(s) to speed up the reloading of the wiring capacity.
After the active phase the internal Pull-up(s) are driving the data bus and there is no need for external Pull-up(s) on the board.

2.3.1.1.1 SRAM Timing for read access

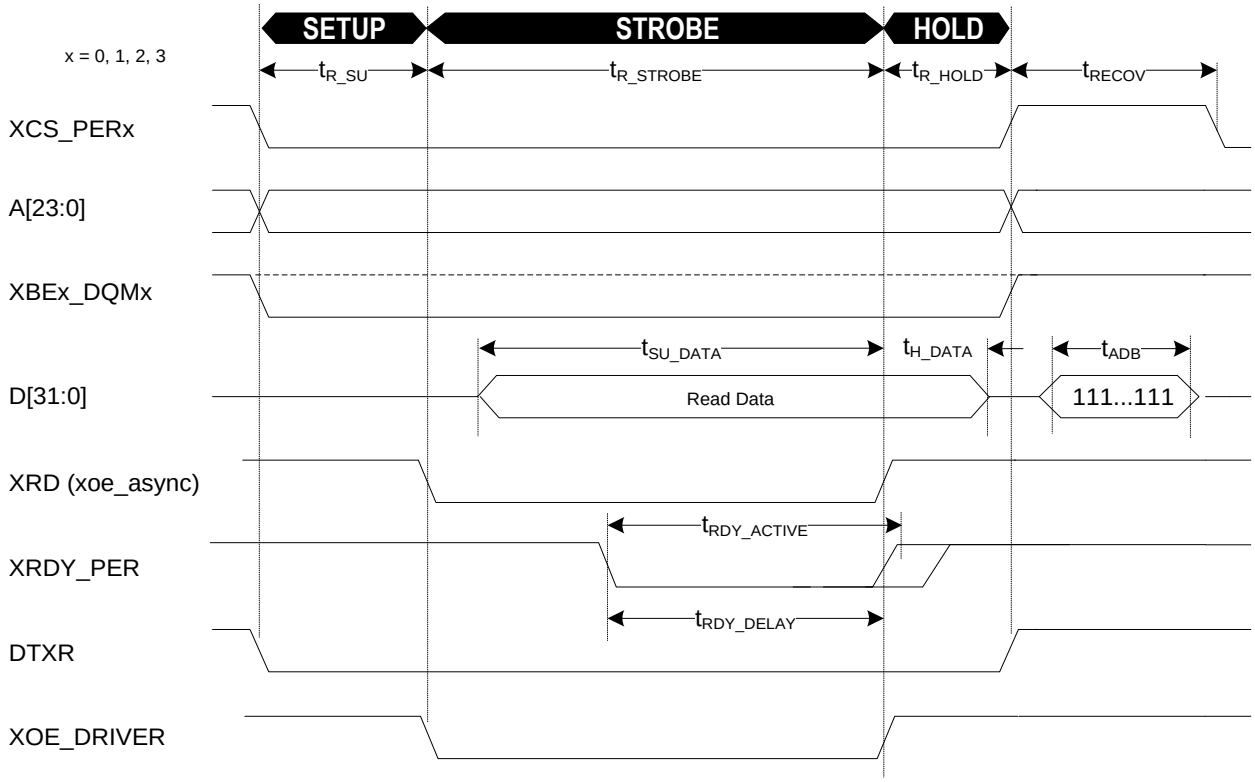

Figure 2-2: SRAM Timing for read access

Table 2-4: EMC Timing (1.8 V)

Parameter	Description	Min	Max	depends on Register	Note
t_{R_SU}	Read Setup-Time	0 Tc – 4.3 ns	15 Tc + 3.5 ns	ASYNC_BANKx.R_SU	1)

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Parameter	Description	Min	Max	depends on Register	Note
t_{R_STROBE}	Read Strobe-Time	1 Tc – 2.4 ns	64 Tc + 3.3 ns	ASYNC_BANKx.R_STROBE	1)
t_{R_HOLD}	Read Hold-Time	1 Tc – 4.2 ns	8 Tc + 3.2 ns	ASYNC_BANKx.R_HOLD	1)
t_{SU_DATA}	Data Setup Time	5.8 ns			
t_{H_DATA}	Data Hold Time	0.0 ns			
t_{RDY_ACTIVE}	Ready Active Time	8.0 ns		ASYNC_BANKx.EW	
t_{RDY_DELAY}	Ready Delay Time	2 Tc + 2.6 ns	3 Tc + 14.7 ns	ASYNC_BANKx.EW	2)
t_{RDY_DELAY}	Ready Delay Time	1 Tc + 4.9 ns	2 Tc + 10.1 ns	ASYNC_BANKx.EW	3)
t_{ADB}	Active data bus	2.4 ns	7.3 ns	EXTENDED_CONFIG.ADB	
t_{RECOV}	Recovery Phase	0 ns	120 ns	RECOV_CONFIG.RECOVx	
Based on	Tc = 8 ns (AHB Clock = 125 MHz); Load-value for Timing = 20 pF Buffer Drive strength = 6 mA IO-Voltage = 1.8 V				

1) BANK_0-4_CONFIG register

2) in ASYNC_BANK0…4 register; Bit 31 – WSM = ‘0’

3) in ASYNC_BANK0…4 register; Bit 31 – WSM = ‘1’

2.3.1.1.2 SRAM Timing for write access

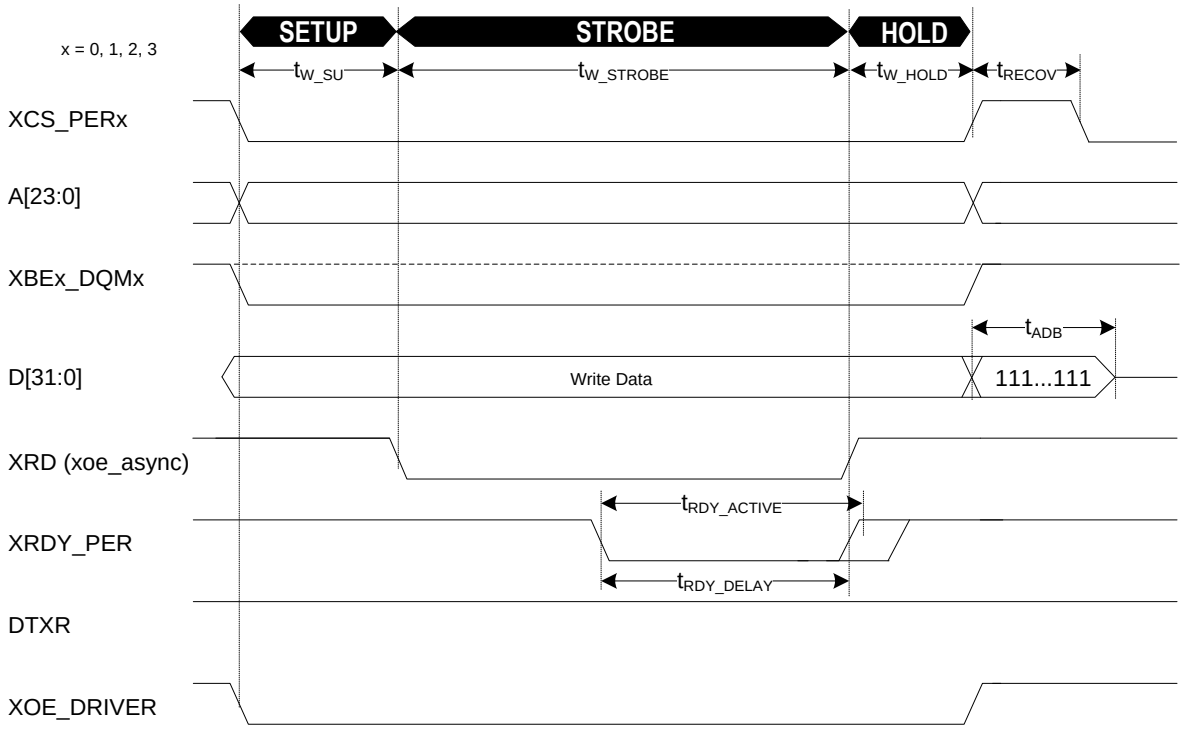

Figure 2-3: SRAM Timing for write access

Table 2-5: SRAM Timing (1.8 V)

Parameter	Description	Min	Max	depends on Register	Note
t_{W_SU}	Write Setup-Time	0 Tc – 3.9 ns	15 Tc + 3.4 ns	ASYNC_BANKx.W_SU	1)
t_{W_STROBE}	Write Strobe-Time	1 Tc + 0.1 ns	64 Tc + 0.9 ns	ASYNC_BANKx.W_STROBE	1)
t_{W_HOLD}	Write Hold-Time	1 Tc – 4.2 ns	8 Tc + 3.3 ns	ASYNC_BANKx.W_HOLD	1)
t_{RDY_ACTIVE}	Ready Active Time	8.0 ns		ASYNC_BANKx.EW	
t_{RDY_DELAY}	Ready Delay Time	2 Tc + 7.5 ns	3 Tc + 13.1 ns	ASYNC_BANKx.EW	2)
t_{RDY_DELAY}	Ready Delay Time	1 Tc + 7.5 ns	2 Tc + 13.1 ns	ASYNC_BANKx.EW	3)
t_{ADB}	Active data bus	3.2 ns	9.5 ns	EXTENDED_CONFIG.ADB	
t_{RECOV}	Recovery Phase	0 ns	120 ns	RECOV_CONFIG.RECOVx	
Based on	Tc = 8 ns (AHB Clock = 125 MHz); Load-value for Timing = 20 pF Buffer Drive strength = 6 mA IO-Voltage = 1.8 V				

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[1)] BANK_0-4_CONFIG register

[2)] in ASYNC_BANK0…4 register; Bit 31 – WSM = ‘0’

[3)] in ASYNC_BANK0…4 register; Bit 31 – WSM = ‘1’

2.3.1.2 SDRAM Timing

The combination of the control signals XCS_DRAM, XRAS_SDRAM, XCAS_SDRAM, XWE_SDRAM and XBEy_DQMy in combination with the Address bus defines SDRAM commands in the following way:

Table 2-6: SDRAM Timing

SDRAM command	XCS_SDRAM	XRAS_SDRAM	XCAS_SDRAM	XWE_SDRAM	XBEy_DQMy	A	Description
COMMAND INHIBIT (NOP)	1	X	X	X	X	X	No operation
NO OPERATION (NOP)	0	1	1	1	X	X	No operation
ACTIVE	0	0	1	1	X	BA/Row	Select bank and activate row
READ	0	1	0	1	1/0	BA/Col	Select bank and column, and start READ Burst
WRITE	0	1	0	0	1/0	BA/Col	Select bank and column, and start WRITE Burst
BURST TERMINATE	0	1	1	0	X	X	Terminate Burst sequence
PRECHARGE	0	0	1	0	X	BA/A10	Deactivate row in bank or banks
AUTO REFRESH	0	0	0	1	X	X	Start auto refresh cycle
LOAD MODE REGISTER	0	0	0	0	X	Op-Code1	Setup of the device-specific configuration register
LOAD EXTENDED MODE REGISTER	0	0	0	0	X	Op-Code2	Setup of the device-specific extended mode configuration register (e.g. mobile SDRAM devices)

X means don’t care.

y = 0, 1, 2, 3

2.3.1.2.1 SDRAM Timing for read access

The output signals are launched with CLK_O_SDRAMx, the input signals are latched in with CLK_I_SDRAM.

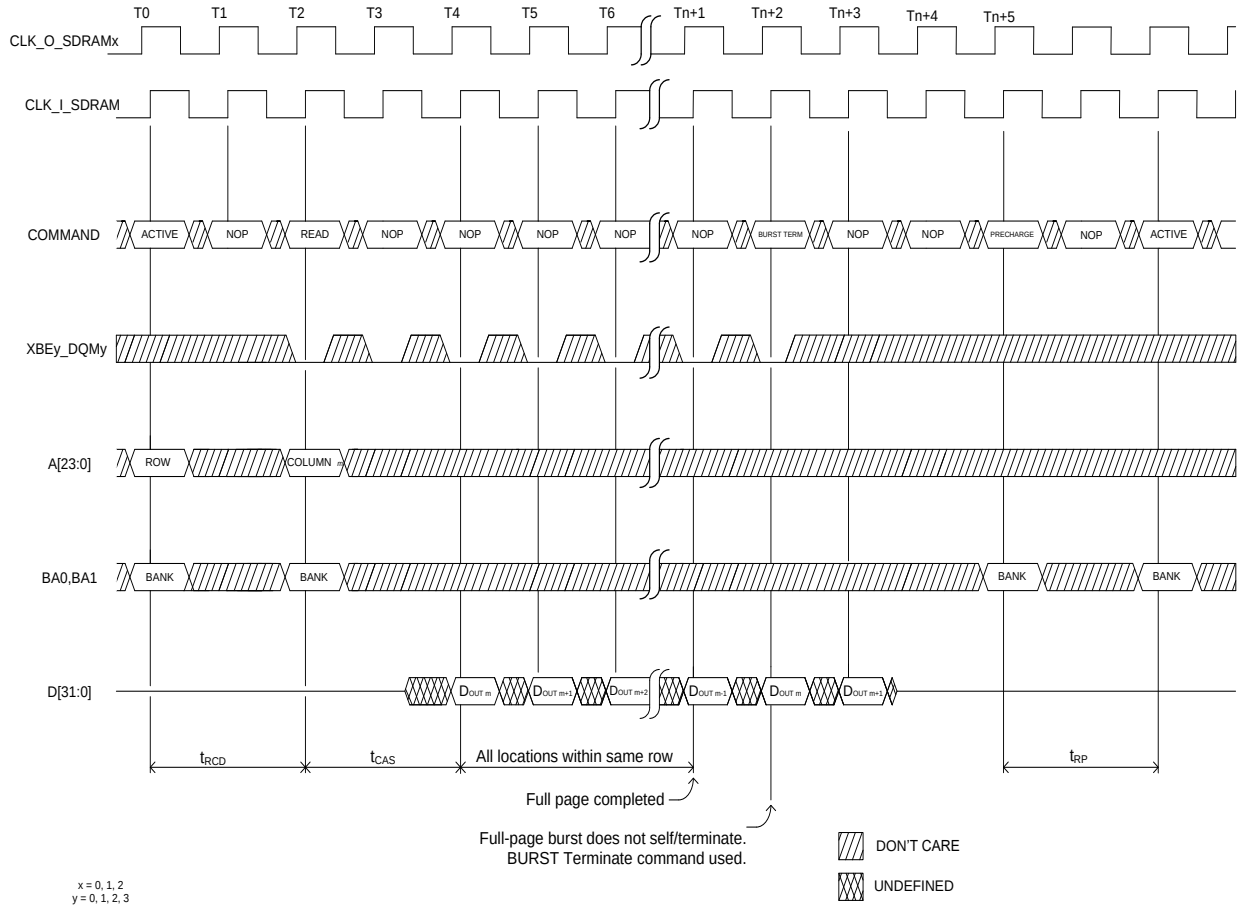

Figure 2-4: SDRAM Timing for read access

Note

The bank signals BA0, BA1 are part of the address bus A. They are presented separately for a better understanding.

Table 2-7: SDRAM Timing for read access (1.8 V)

Parameter	Description	Min	Max	depends on Register	Note
t_{RCD}	RAS to CAS delay	16 ns	32 ns	EXTENDED_CONFIG.TRCD	
t_{CAS}	CAS Latency	16 ns	24 ns	SDRAM_CONFIG.CL	
t_{RP}	Row precharge latency	24 ns	24 ns		
t_{DS}	Data Setup Time	0.8 ns			CLK_I_SDRAM
t_{DH}	Data Hold Time	1.3 ns			CLK_I_SDRAM
Based on	Tc = 8 ns (AHB Clock = 125 MHz); Load-value for Timing = 20 pF Buffer Drive strength = 6 mA IO-Voltage = 1.8 V				

Setup and hold times for address, command and data are the same as with write access. They can be found in the following chapter.

2.3.1.2.2 SDRAM Timing for write access

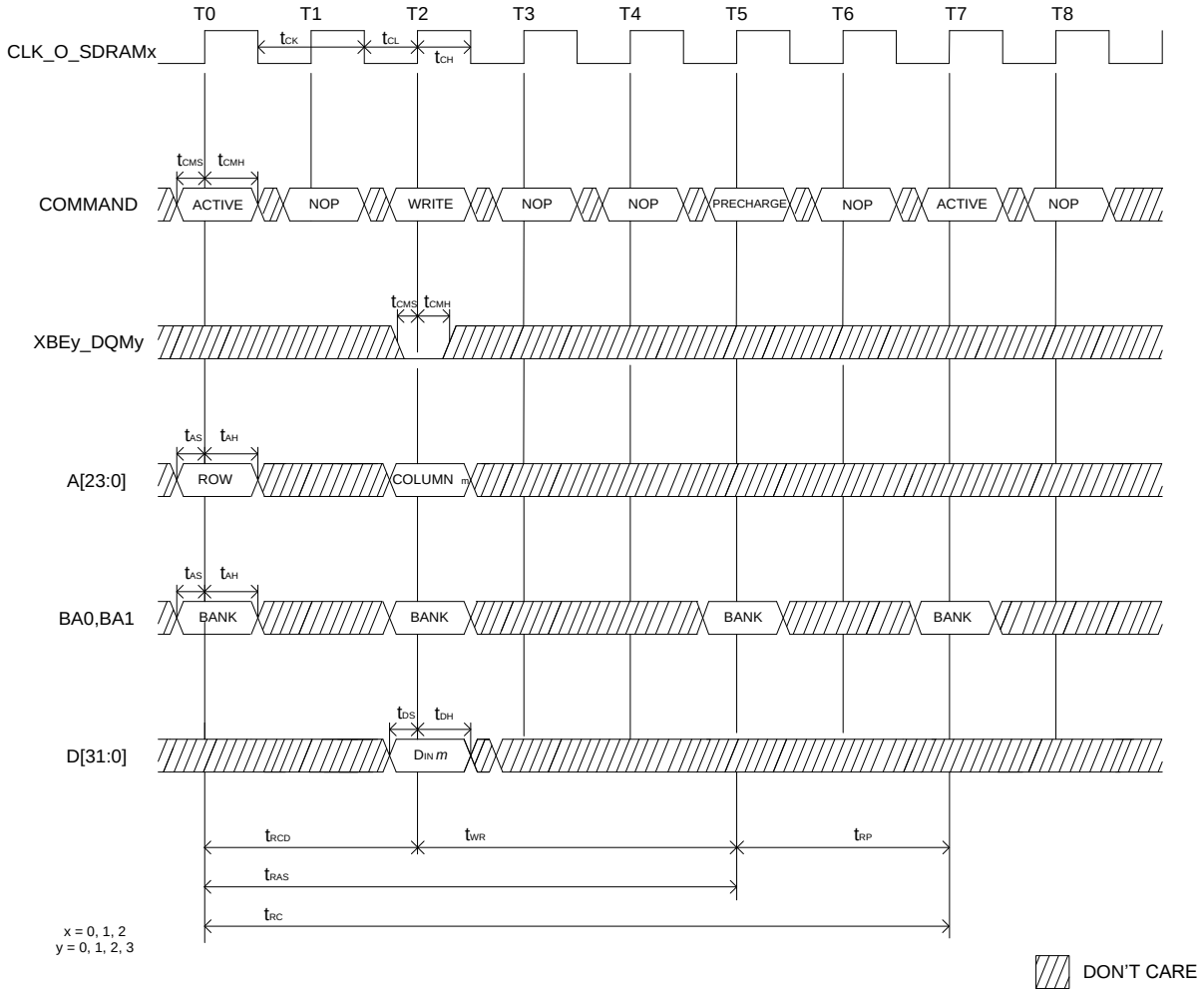

Figure 2-5: SDRAM Timing for write access

Note

The bank signals BA0, BA1 are part of the address bus A. They are presented separately for a better understanding

Table 2-8: SDRAM Timing for write access (1.8V)

Parameter	Description	Min	Max	depends on Register	Note
t_{CK}	Clock Period	7.9 ns	8.1 ns	-	
t_{CMS}	Command Setup Time	5.0 ns	-	-	
t_{CMH}	Command Hold Time	1.8 ns	-	-	
t_{AS}	Address Setup Time	5.0 ns	-	-	
t_{AH}	Address Hold Time	1.8 ns	-	-	

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t_{DS}	Data Setup Time	4.4 ns	-	-	
t_{DH}	Data Hold Time	1.6 ns	-	-	
t_{RCD}	RAS to CAS delay	16 ns	40 ns	EXTENDED_CONFIG.TRCD + 1	
t_{RAS}	Row Address Strobe	$t_{RCD} + t_{WR}$	1)		
t_{RC}	ROW cycle Time	$t_{RCD} + t_{WR} + t_{RP}$	-	-	
t_{WR}	Write to Precharge Time	16 ns	1)	-	
t_{RP}	Row precharge latency	24 ns	24 ns	-	
Based on	Tc = 8 ns (AHB Clock = 125 MHz); Load-value for Timing = 20 pF Buffer Drive strength = 6 mA IO-Voltage = 1.8 V				

1) Depends on Refresh Cycle Time

2.3.2 XHIF Timing

2.3.2.1 Separate RD/WR

The following figure shows the timing, when the External Host initiates a **Read Access**.

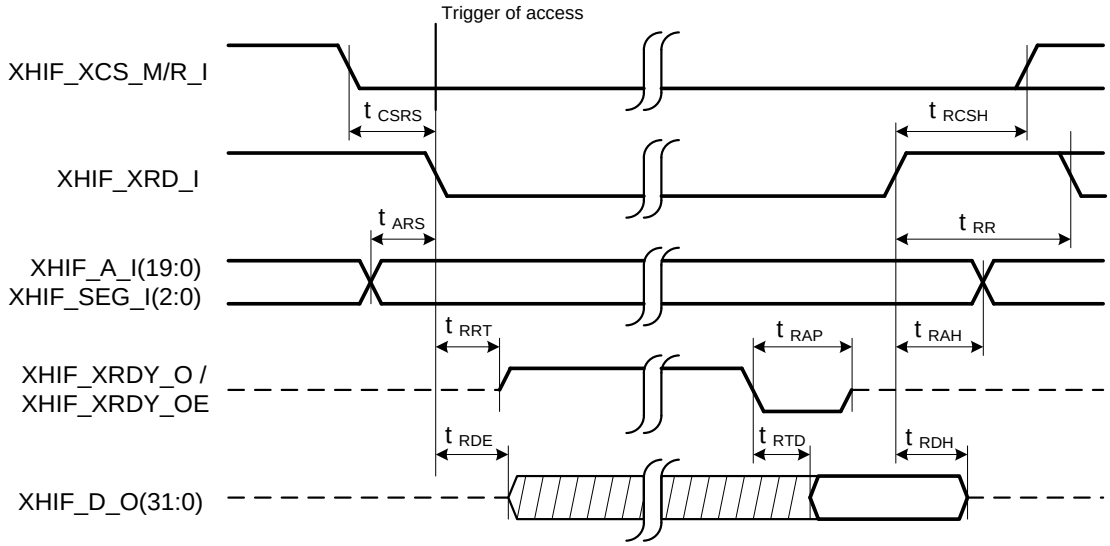


Figure 2-6: XHIF Read Access

Table 2-9: Host Interface Timing for read (1.8 V)

Parameter	Description	Min	Max
t_{CSRS}	Chip select asserted to read pulse asserted delay	4.0 ns[1)]	
t_{ARS}	Address valid to read pulse asserted setup time	3.5 ns	
t_{RRT}	Read pulse asserted to ready deasserted delay	6.1 ns	20.8 ns

t_{RDE}	Read pulse asserted to data enable delay	6.1 ns	21.1 ns
t_{RAP}	Ready active pulse width	3.2 ns	10.8 ns
t_{RTD}	Ready asserted to data valid delay		3.6 ns
t_{RCSH}	Read pulse deasserted to chip select deasserted delay	3.2 ns[2)]	
t_{RAH}	Address valid to read pulse deasserted hold time	3.6 ns	
t_{RDH}	Data valid/enable to read pulse deasserted hold time	4.1 ns	21.5 ns
t_{RR}	Read recovery time	12.6 ns	
Based on	Tc = 8 ns (AHB Clock = 125 MHz); Load-value for Timing = 20 pF Buffer Drive strength = 8 mA IO-Voltage = 1.8 V		

[1)] If $t_{CSRS} < 0$, t_{ARS}, t_{RRT} and t_{RDE} are related to the falling edge of XHIF_XCS

[2)] If $t_{RCSH} < 0$, t_{RAH} and t_{RDH} are related to the rising edge of XHIF_XCS

Table 2-10: Host Interface Timing for read (3.3 V)

Parameter	Description	Min	Max
t_{CSRS}	Chip select asserted to read pulse asserted delay	3.7 ns[1)]	
t_{ARS}	Address valid to read pulse asserted setup time	4.0 ns	
t_{RRT}	Read pulse asserted to ready deasserted delay	4.2 ns	14.4 ns
t_{RDE}	Read pulse asserted to data enable delay	4.4 ns	14.7 ns
t_{RAP}	Ready active pulse width	5.2 ns	9.6 ns
t_{RTD}	Ready asserted to data valid delay		2.2 ns
t_{RCSH}	Read pulse deasserted to chip select deasserted delay	3.2 ns[2)]	
t_{RAH}	Address valid to read pulse deasserted hold time	4.1 ns	
t_{RDH}	Data valid/enable to read pulse deasserted hold time	3.7 ns	15.4 ns
t_{RR}	Read recovery time	13.1 ns	
Based on	Tc = 8 ns (AHB Clock = 125 MHz); Load-value for Timing = 20 pF Buffer Drive strength = 8 mA IO-Voltage = 3.3 V		

[1)] If $t_{CSRS} < 0$, t_{ARS}, t_{RRT} and t_{RDE} are related to the falling edge of XHIF_XCS

[2)] If $t_{RCSH} < 0$, t_{RAH} and t_{RDH} are related to the rising edge of XHIF_XCS

The following figure shows the timing, when the External Host initiates a **Write Access**:

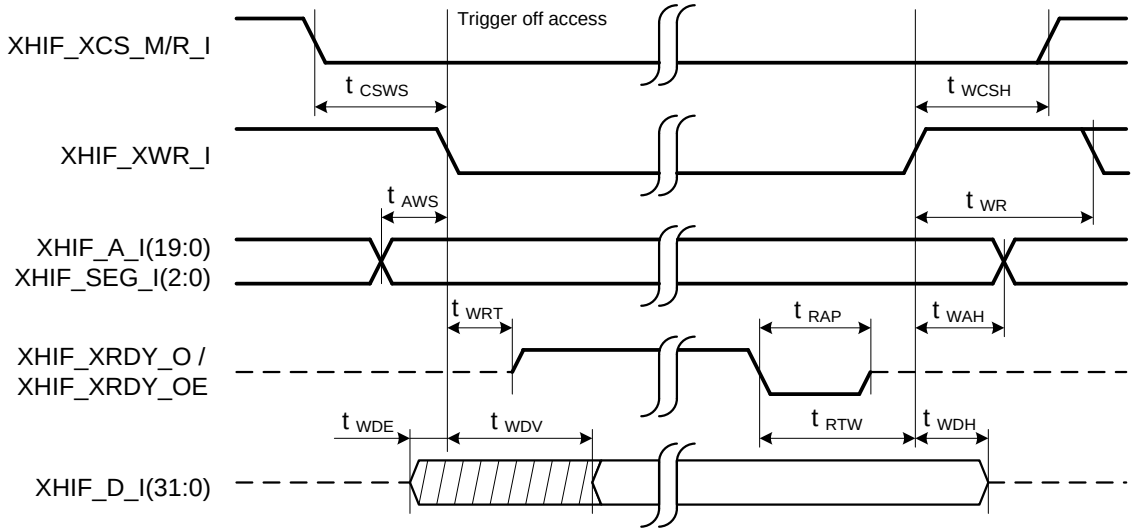


Figure 2-7: XHIF Write Access

Table 2-11: Host Interface Timing for write (1.8 V)

Parameter	Description	Min	Max
t_{CSWS}	Chip select asserted to write pulse asserted delay	2.1 ns[1)]	
t_{AWS}	Address valid to write pulse asserted setup time	3.1 ns	
t_{WRT}	Write pulse asserted to ready deasserted delay	6.0 ns	21.1 ns
t_{WDE}	Write pulse asserted to data enable setup	0 ns	t.b.d ns[3)]
t_{WDV}	Write pulse asserted to data valid delay		15.2 ns
t_{RAP}	Ready active pulse width	3.2 ns	10.8 ns
t_{WCSH}	Write pulse deasserted to chip select deasserted delay	3.0 ns[2)]	
t_{WAH}	Address valid to write pulse deasserted hold time	3.4 ns	
t_{RTW}	Ready asserted to write pulse deasserted delay	0 ns	
t_{WDH}	Data valid/enabled to read pulse deasserted hold time	3.4 ns[2)]	
t_{WR}	Write recovery time	12.7 ns	
Based on	Tc = 8 ns (AHB Clock = 125 MHz); Load-value for Timing = 20 pF Buffer Drive strength = 8 mA IO-Voltage = 1.8 V		

[1)] If $t_{CSWS} < 0$, t_{AWS}, t_{WRT} and t_{WDE} are related to the falling edge of XHIF_XCS

[2)] If $t_{WCSH} < 0$, t_{WAH} and t_{WDH} are related to the rising edge of XHIF_XCS

[3)] t_{WDE} may have any value, as long as it is assured that there is 1 idle cycle (of the XHIF clock period) guaranteed between the end of the preceding access and the start of the current access (indicated by the falling edge of XCS/XWR). Within this idle cycle no access is allowed at all.

Table 2-12: Host Interface Timing for write (3.3 V)

Parameter	Description	Min	Max
t_{CSWS}	Chip select asserted to write pulse asserted delay	2.4 ns[1)]	
t_{AWS}	Address valid to write pulse asserted setup time	4.0 ns	
t_{WRT}	Write pulse asserted to ready deasserted delay	4.2 ns	14.7 ns
t_{WDE}	Write pulse asserted to data enable setup	0 ns	t.b.d ns[3)]
t_{WDV}	Write pulse asserted to data valid delay		15.2 ns
t_{RAP}	Ready active pulse width	5.2 ns	9.6 ns
t_{WCSH}	Write pulse deasserted to chip select deasserted delay	3.0 ns[2)]	
t_{WAH}	Address valid to write pulse deasserted hold time	4.0 ns	
t_{RTW}	Ready asserted to write pulse deasserted delay	0 ns	
t_{WDH}	Data valid/enabled to read pulse deasserted hold time	3.9 ns[2)]	
t_{WR}	Write recovery time	13.2 ns	
Based on	Tc = 8 ns (AHB Clock = 125 MHz); Load-value for Timing = 20 pF Buffer Drive strength = 8 mA IO-Voltage = 3.3 V		

[1)] If $t_{CSWS} < 0$, t_{AWS}, t_{WRT} and t_{WDE} are related to the falling edge of XHIF_XCS

[2)] If $t_{WCSH} < 0$, t_{WAH} and t_{WDH} are related to the rising edge of XHIF_XCS

[3)] t_{WDE} may have any value, as long as it is assured that there is 1 idle cycle (of the XHIF clock period) guaranteed between the end of the preceding access and the start of the current access (indicated by the falling edge of XCS/XWR). Within this idle cycle no access is allowed at all.

2.3.2.2 Common RD/WR

The following figure shows the timing, when the External Host initiates a **Common Read Access**.

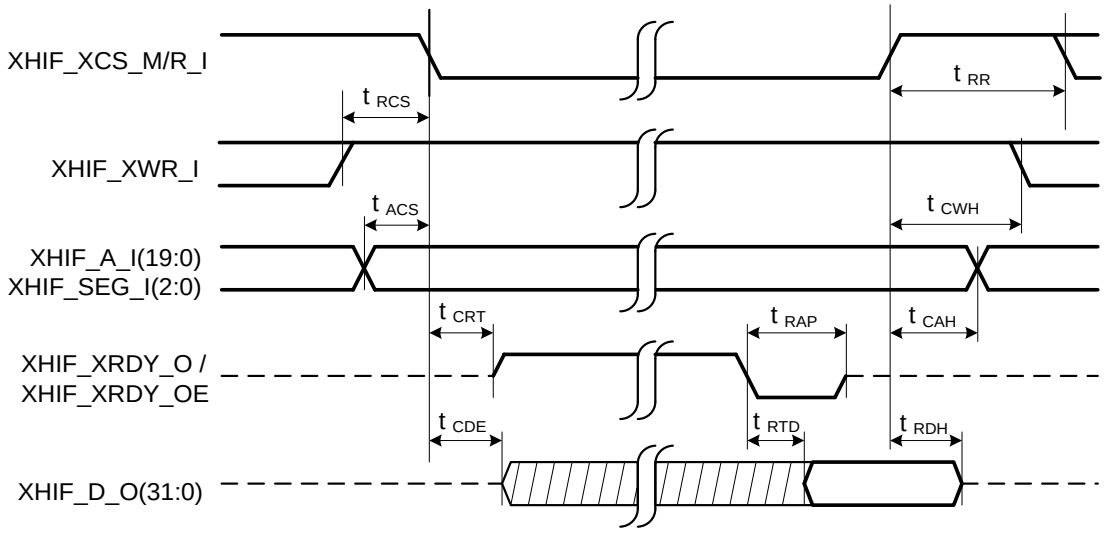


Figure 2-8: XHIF Common Read Access

Table 2-13: Host Interface Timing for common read (1.8 V)

Parameter	Description	Min	Max
t_{RCS}	Write signal deasserted to chip select asserted delay	10.3 ns	
t_{ACS}	Address valid to chip select asserted setup time	3.6 ns	
t_{CRT}	Chip select asserted to ready deasserted delay	4.1 ns	21.1 ns
t_{CDE}	Chip select asserted to data enable delay	4.2 ns	21.1 ns
t_{RAP}	Ready active pulse width	3.2 ns	10.8 ns
t_{RTD}	Ready asserted to data valid delay		3.6 ns
t_{CWH}	Chip select deasserted to write signal asserted delay	4.3 ns	
t_{CAH}	Address valid to chip select deasserted hold time	3.1 ns	
t_{RDH}	Data valid/enable to chip select deasserted hold time	4.1 ns	21.5 ns
t_{RR}	Read recovery time	12.2 ns	
Based on	Tc = 8 ns (AHB Clock = 125 MHz); Load-value for Timing = 20 pF Buffer Drive strength = 8 mA IO-Voltage = 1.8 V		

Table 2-14: Host Interface Timing for common read (3.3 V)

Parameter	Description	Min	Max
t_{RCS}	Write signal deasserted to chip select asserted delay	6.4 ns	
t_{ACS}	Address valid to chip select asserted setup time	4.1 ns	
t_{CRT}	Chip select asserted to ready deasserted delay	3.2 ns	14.7 ns
t_{CDE}	Chip select asserted to data enable delay	3.5 ns	14.7 ns
t_{RAP}	Ready active pulse width	5.2 ns	9.6 ns
t_{RTD}	Ready asserted to data valid delay		2.2 ns
t_{CWH}	Chip select deasserted to write signal asserted delay	4.1 ns	
t_{CAH}	Address valid to chip select deasserted hold time	3.6 ns	
t_{RDH}	Data valid/enable to chip select deasserted hold time	3.7 ns	15.4 ns
t_{RR}	Read recovery time	12.7 ns	
Based on	Tc = 8 ns (AHB Clock = 125 MHz); Load-value for Timing = 20 pF Buffer Drive strength = 8 mA IO-Voltage = 3.3V		

The following figure shows the timing, when the External Host initiates a **Common Write Access**:

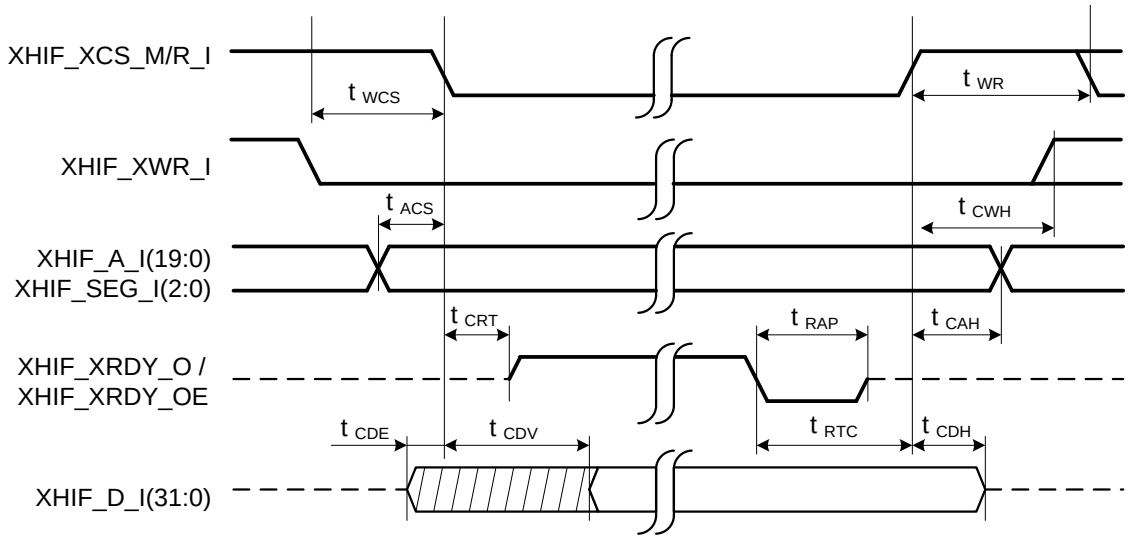


Figure 2-9: XHIF Common Write Access

Table 2-15: Host Interface Timing for common write (1.8 V)

Parameter	Description	Min	Max
t_{WCS}	Write signal asserted to chip select setup time	3.4 ns[1)]	
t_{ACS}	Address valid to chip select asserted setup time	3.6 ns	
t_{CRT}	Chip select asserted to ready deasserted delay	4.1 ns	21.1 ns
t_{CDE}	Chip select asserted to data enable setup	-2.5 ns	3.8 ns[2)]
t_{CDV}	Chip select asserted to data valid delay		15.0 ns
t_{RAP}	Ready active pulse width	3.2 ns	10.8 ns
t_{CWH}	Write signal deasserted to chip select deasserted delay	2.7 ns	
t_{CAH}	Address valid to chip select deasserted hold time	0 ns	
t_{RTC}	Ready asserted to chip select deasserted delay	0 ns	
t_{CDH}	Data valid/enabled to chip select deasserted hold time	0 ns[2)]	
t_{WR}	Write recovery time	12.2 ns	
Based on	Tc = 8 ns (AHB Clock = 125 MHz); Load-value for Timing = 20 pF Buffer Drive strength = 8 mA IO-Voltage = 1.8 V		

[1)] It is important to meet the setup timing of the Write signals; otherwise the XHIF module is driving the data bus.

[2)] t_{CDE} may have any value, as long as it is assured, that there is 1 idle cycle (of the XHIF clock period) guaranteed between the end of the preceding access and the start of the current access (indicated by the falling edge of XHIF_XCS). Within this idle cycle no access is allowed at all.

Table 2-16: Host Interface Timing for common write (3.3 V)

Parameter	Description	Min	Max
t_{WCS}	Write signal asserted to chip select setup time	3.3 ns[1)]	
t_{ACS}	Address valid to chip select asserted setup time	4.1 ns	
t_{CRT}	Chip select asserted to ready deasserted delay	3.7 ns	14.7 ns
t_{CDE}	Chip select asserted to data enable setup	-2.5 ns	4.3 ns[2)]
t_{CDV}	Chip select asserted to data valid delay		15.0 ns
t_{RAP}	Ready active pulse width	5.2 ns	9.6 ns
t_{CWH}	Write signal deasserted to chip select deasserted delay	3.2 ns	
t_{CAH}	Address valid to chip select deasserted hold time	0 ns	
t_{RTC}	Ready asserted to chip select deasserted delay	0 ns	
t_{CDH}	Data valid/enabled to chip select deasserted hold time	0 ns[2)]	
t_{WR}	Write recovery time	12.7 ns	
Based on	Tc = 8 ns (AHB Clock = 125 MHz); Load-value for Timing = 20 pF Buffer Drive strength = 8 mA IO-Voltage = 3.3V		

[1)] It is important to meet the setup timing of the Write signals; otherwise the XHIF module is driving the data bus.

[2)] t_{CDE} may have any value, as long as it is assured, that there is 1 idle cycle (of the XHIF clock period) guaranteed between the end of the preceding access and the start of the current access (indicated by the falling edge of XHIF_XCS). Within this idle cycle no access is allowed at all.

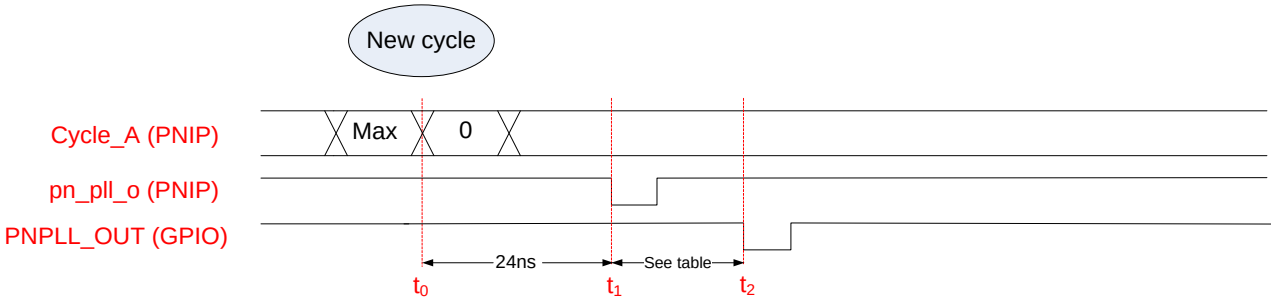
2.3.3 PNPLL Timing

A total of 21 PNPLL signals are sent to the ERTEC 200P top level from the PN-IP. Of these signals, the **nine** output signals PNPLL_out(8..0) can be connected to ext. pins over GPIOs. PNPLL_Extin can also be connected as an input signal from an ext.pin to the PNPLL over a GPIO.

One of the nine output signals PNPLL_out(8..0) can be used as SyncOut for measuring the synchronism of individual nodes in a network topology.

Multiplexers and GPIOs must be set accordingly on the ERTEC 200P top level.

PNPLL_OUT can be measured at the selected GPIO pin; the signal is generated as follows:



t_0: Start of cycle, i.e. the time at which a clock edge switches the cycle timer from its maximum value to its minimum value.

t_1: pn_pll_o is output by PN-IP (output signal to entity).

t_2: The signal PNPLL_OUT appears at the external GPIO pin

Figure 2-10: PNPLL Timing

This produces the following time delay in the PN-IP:

	Time	Explanation	Min/Max (ns)
PN-IP	$t_0 \rightarrow t_1$	Time from Cycle_A transition until the internal PN-IP flip-flop of pn_pll_o(0) changes from 1 to 0.	**24 ns** *(exactly three 8 ns clock cycles)*
ERTEC 200P	$t_1 \rightarrow t_2$	Output_delay of one the following PNPLL output signals from the PN-IP to the GPIO pin.	See Table 2-17

Table 2-17: PNPLL Timing

Signal (Input)	Ports	Alternate Function	Input_delay		Load (pF) Min / Max	Reference	Functional characteristics
			-min	-max			
PNPLL_EXTIN_A	GPIO9_INT	A	18.2 ns	30.9 ns	-	CLK_SYS	asynchronous
	GPIO_23	B	18.0 ns	30.9 ns	-	CLK_SYS	asynchronous
Signal (Output)			**Clock-to-Output_delay**			**Reference**	
			-min	**-max**			
PNPLL_OUT0	GPIO0_INT	A	3.5 ns	10.0 ns	20	CLK_SYS	asynchronous
	XHIF_XWR	C	3.0 ns	7.8 ns	20	CLK_SYS	asynchronous
PNPLL_OUT1	GPIO1_INT	A	3.5 ns	9.4 ns	20	CLK_SYS	asynchronous
	XHIF_XRD	C	3.3 ns	9.2 ns	20	CLK_SYS	asynchronous
PNPLL_OUT2	GPIO2_INT	A	3.7 ns	10.1 ns	20	CLK_SYS	asynchronous
	XHIF_XCS_R.	C	3.9 ns	10.5 ns	20	CLK_SYS	asynchronous
PNPLL_OUT3	GPIO3_INT	A	3.6 ns	9.8 ns	20	CLK_SYS	asynchronous
	XHIF_XCS_M	C	2.9 ns	7.9 ns	20	CLK_SYS	asynchronous
PNPLL_OUT4	GPIO4_INT	A	3.8 ns	10.6 ns	20	CLK_SYS	asynchronous
	XHIF_XBE0	C	2.9 ns	7.6 ns	20	CLK_SYS	asynchronous
PNPLL_OUT5	GPIO5_INT	A	3.7 ns	10.1 ns	20	CLK_SYS	asynchronous
	XHIF_XBE1	C	2.8 ns	7.4 ns	20	CLK_SYS	asynchronous
PNPLL_OUT6	GPIO6_INT	A	3.1 ns	7.6 ns	20	CLK_SYS	asynchronous
	GPIO29	C	2.8 ns	8.3 ns	20	CLK_SYS	asynchronous
PNPLL_OUT7	GPIO7_INT	A	3.5 ns	8.8 ns	20	CLK_SYS	asynchronous
	GPIO30	C	2.8 ns	7.3 ns	20	CLK_SYS	asynchronous
PNPLL_OUT8	GPIO8_INT	A	3.6 ns	9.5 ns	20	CLK_SYS	asynchronous
	GPIO31	C	2.8 ns	7.3 ns	20	CLK_SYS	asynchronous

Note: PNPLL_EXTIN_A input delay values contain 16.0 ns to 24.0 ns delay caused by synchronization mechanisms

Table 2-18: Timing for time synchronization

Signal (Input)	Ports	Alternate Function	Input_delay		Load (pF) Min / Max	Reference	Functional characteristics
			-min	-max			
PNPLL_EXTIN_Time	GPIO12_INT	A	18.1 ns	30.2 ns	-	CLK_SYS	asynchronous
Signal (Output)			**Clock-to-Output_delay**				
			-min	**-max**			
PNPLL_Time_Out	GPIO11_INT	A	3.5 ns	9.8 ns	20	CLK_SYS	asynchronous
	GPIO28	C	3.5 ns	9.5 ns	20	CLK_SYS	asynchronous

Note: PNPLL_EXTIN_TIME input delay values contain 16.0 ns to 24.0 ns delay caused by synchronization mechanisms

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Table 2-19: PNPLL triggered by internal sources

Signal (Input)	Source	-	delay		Load (pF) Min / Max	Reference	Functional characteristics
			-min	-max			
PNPLL_EXTIN	ISOSYNC1PLL	-	17.0 ns	27.5 ns	-	CLK_SYS	asynchronous
	ISOSYNC2PLL	-	17.1 ns	27.1 ns	-	CLK_SYS	asynchronous
	PBUSPPLL						

Note: PNPLL_EXTIN delay values contain 16.0 ns to 24.0 ns delay caused by synchronization mechanisms

2.3.4 Peripheral Interface Timing

2.3.4.1 Local GPIO (Parallel) Timing

The GPIO interface is asynchronous to external signals. External inputs will be synchronized internally. All inputs have no timing relation from an external clock to internal clock of ERTEC 200P. All outputs have no timing relation from internal clock of ERTEC 200P to an external clock.

Table 2-20: Local GPIO (Parallel) Timing (1.8 V)

Symbol	Description	Min	Max	Unit	Note
T_{din}	Runtime of Input signals	1.9	10.8	ns	
T_{dout}	Runtime of Output signals	3.1	12.2	ns	
$T_{din\ skew}$	Skew of Input signals		4.9	ns	
$T_{dout\ skew}$	Skew of Output signals		3.8	ns	
Based on	Buffer Drive strength = 8mA IO-Voltage = 1.8 V				

Table 2-21: Local GPIO (Parallel) Timing (3.3 V)

Symbol	Description	Min	Max	Unit	Note
T_{din}	Runtime of Input signals	1.7	10.4	ns	
T_{dout}	Runtime of Output signals	2.3	7.2	ns	
$T_{din\ skew}$	Skew of Input signals		6.3	ns	
$T_{dout\ skew}$	Skew of Output signals		2.4	ns	
Based on	Buffer Drive strength = 8mA IO-Voltage = 3.3 V				

2.3.4.2 Local SPI (Serial) Timing

The frequency of SSPCLK (base frequency for SPI macro): f_{SSPCLK} = 125 MHz.

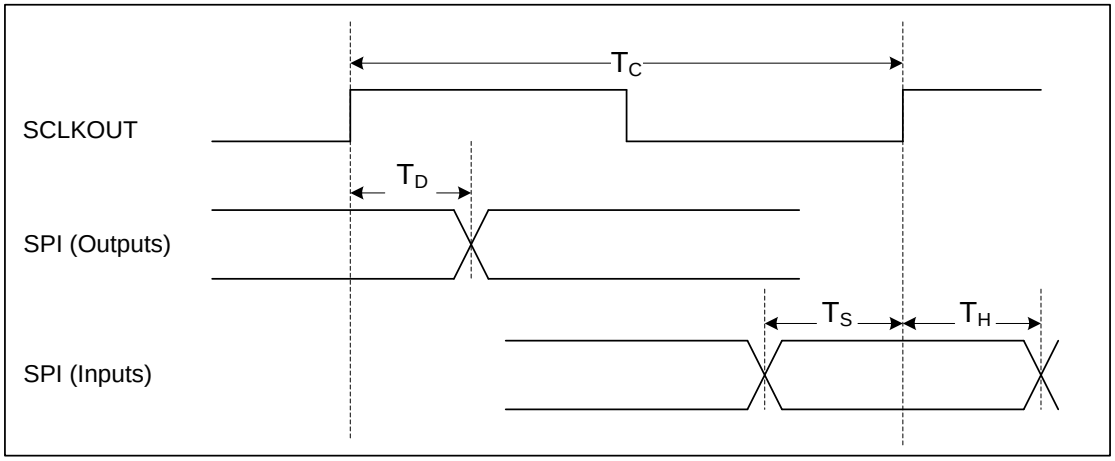

Figure 2-11: SPI (Serial) Timing

Table 2-22: Local SPI1 (Serial) Timing (1.8 V)

Symbol	Parameter	Min.	Max.	Unit	Note
T_C	Baudrate	31.25	-	ns	Master
T_D	Valid delay	-0.5	0.8	ns	1)
T_S	Setup Time	14.4	-	ns	2)
T_H	Hold Time	0	-	ns	2)
Based on	Buffer Drive strength = 8mA IO-Voltage = 1.8 V				

1) C_L = 20 pF

2) T_s, T_h > 1 x 125 MHz period; Inputs are synchronized with APB clock (F_{SSPCLK}).

Table 2-23: Local SPI1 (Serial) Timing (3.3 V)

Symbol	Parameter	Min.	Max.	Unit	Note
T_C	Baudrate	31.25	-	ns	Master
T_D	Valid delay	-0.1	1.3	ns	1)
T_S	Setup Time	9.8	-	ns	2)
T_H	Hold Time	0	-	ns	2)
Based on	Buffer Drive strength = 8mA IO-Voltage = 3.3 V				

1) C_L = 20 pF

2) T_s, T_h > 1 x 125 MHz period; Inputs are synchronized with APB clock (F_{SSPCLK}).

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Table 2-24: Local SPI2 (Serial) Timing (1.8 V)

Symbol	Parameter	Min.	Max.	Unit	Note
T_C	Baudrate	31.25	-	ns	Master
T_D	Valid delay	-0.3	1.3	ns	1)
T_S	Setup Time	14.3	-	ns	2)
T_H	Hold Time	0	-	ns	2)
Based on	Buffer Drive strength = 8mA IO-Voltage = 1.8 V				

1) C_L = 20 pF

2) T_s, T_h > 1 x 125 MHz period; Inputs are synchronized with APB clock (F_{SSPCLK}).

Table 2-25: Local SPI2 (Serial) Timing (3.3 V)

Symbol	Parameter	Min.	Max.	Unit	Note
T_C	Baudrate	31.25	-	ns	Master
T_D	Valid delay	0.2	1.5	ns	1)
T_S	Setup Time	9.9	-	ns	2)
T_H	Hold Time	0	-	ns	2)
Based on	Buffer Drive strength = 8mA IO-Voltage = 3.3 V				

1) C_L = 20 pF

2) T_s, T_h > 1 x 125 MHz period; Inputs are synchronized with APB clock (F_{SSPCLK}).

2.3.5 SPI Timing

The frequency of SSPCLK (base frequency for SPI macro): f_{SSPCLK} = 125 MHz.

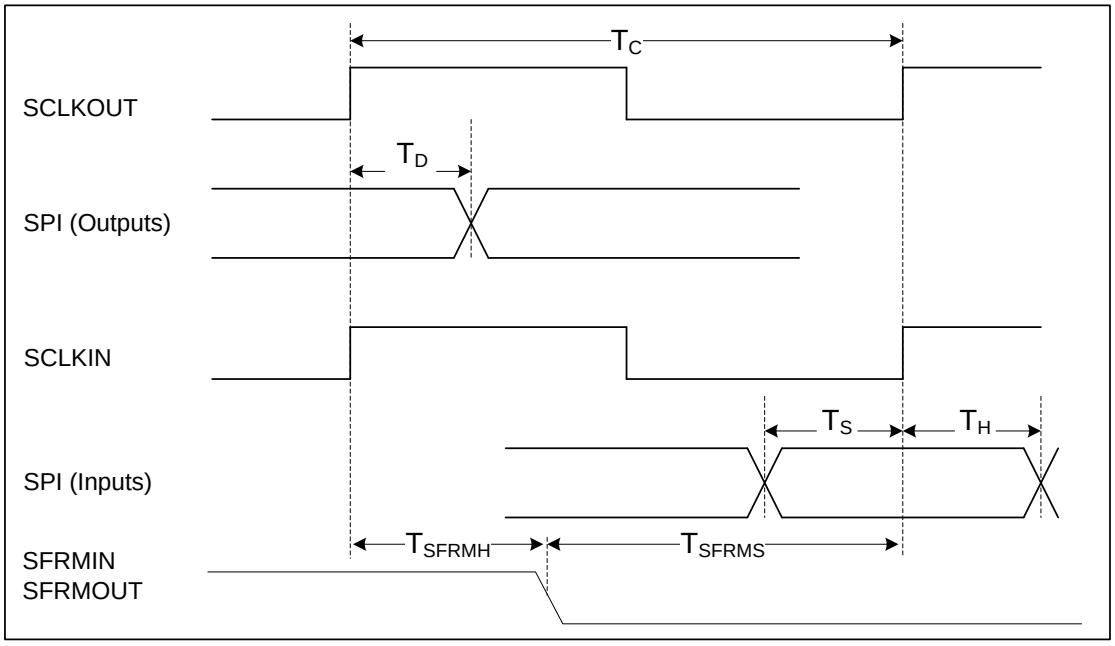

Figure 2-12: SPI Timing

Table 2-26: SPI1 Timing via GPIO Alternate Function A

Symbol	Parameter	Min.	Max.	Unit	Note
T_C	Baudrate	25	-	ns	Master
		150	-	ns	Slave[3)]
T_D	Valid delay	-1.1	0.6	ns	Master[1)]
		19.5	34.5	ns	Slave[3)]
T_S	Setup Time	10.7	-	ns	Master[2)]
		-15.7	-	ns	Slave[2), 3)]
T_H	Hold Time	-3.6	-	ns	Master[2)]
		26.2	-	ns	Slave[2), 3)]
T_{SFRMS}	SFRMIN Setup Time	18.8	-	ns	
T_{SFRMH}	SFRMIN Hold Time	7.9	-	ns	
Based on	Buffer Drive strength = 8 mA IO-Voltage = 3.3 V				

[1)] C_L = 20 pF

[2)] T_s, T_h > 1 x 125 MHz period; Inputs are synchronized with APB clock (F_{SSPCLK}).

[3)] Slave-Mode : SCLK_IN is synchronized in (2 internal clocks)

Table 2-27: SPI1 Timing via GPIO Alternate Function C

Symbol	Parameter	Min.	Max.	Unit	Note
T_C	Baudrate	25	-	ns	Master
		150	-	ns	Slave[3)]
T_D	Valid delay	-0.9	1.7	ns	Master[1)]
		21.8	38.9	ns	Slave[3)]
T_S	Setup Time	14.3	-	ns	Master[2)]
		-15.8	-	ns	Slave[2), 3)]
T_H	Hold Time	-5.2	-	ns	Master[2)]
		26.1	-	ns	Slave[2), 3)]
T_{SFRMS}	SFRMIN Setup Time	19.3	-	ns	
T_{SFRMH}	SFRMIN Hold Time	7.0	-	ns	
Based on	Buffer Drive strength = 8 mA IO-Voltage = 3.3 V				

[1)] C_L = 20 pF

[2)] T_s, T_h > 1 x 125 MHz period; Inputs are synchronized with APB clock (F_{SSPCLK}).

[3)] Slave-Mode : SCLK_IN is synchronized in (2 internal clocks)

Table 2-28: SPI2 Timing via GPIO Alternate Function A

Symbol	Parameter	Min.	Max.	Unit	Note
T_C	Baudrate	25	-	ns	Master
		150	-	ns	Slave[3)]
T_D	Valid delay	-1.3	0.3	ns	Master[1)]
		20.0	35.7	ns	Slave[3)]
T_S	Setup Time	11.5	-	ns	Master[2)]
		-15.7	-	ns	Slave[2), 3)]
T_H	Hold Time	-3.9	-	ns	Master[2)]
		26.0	-	ns	Slave[2), 3)]
T_{SFRMS}	SFRMIN Setup Time	18.1	-	ns	
T_{SFRMH}	SFRMIN Hold Time	7.7	-	ns	
Based on	Buffer Drive strength = 8 mA IO-Voltage = 3.3 V				

[1)] C_L = 20 pF

[2)] T_s, T_h > 1 x 125 MHz period; Inputs are synchronized with APB clock (F_{SSPCLK}).

[3)] Slave-Mode : SCLK_IN is synchronized in (2 internal clocks)

Table 2-29: SPI2 Timing via GPIO Alternate Function C

Symbol	Parameter	Min.	Max.	Unit	Note
T_C	Baudrate	25	-	ns	Master
		150	-	ns	Slave[3)]
T_D	Valid delay	-1.1	0.6	ns	Master[1)]
		20.1	36.2	ns	Slave[3)]
T_S	Setup Time	11.5	-	ns	Master[2)]
		-16.0	-	ns	Slave[2), 3)]
T_H	Hold Time	-3.6	-	ns	Master[2)]
		27.2	-	ns	Slave[2), 3)]
T_{SFRMS}	SFRMIN Setup Time	18.6	-	ns	
T_{SFRMH}	SFRMIN Hold Time	7.6	-	ns	
Based on	Buffer Drive strength = 8 mA IO-Voltage = 3.3 V				

[1)] C_L = 20 pF

[2)] T_s, T_h > 1 x 125 MHz period; Inputs are synchronized with APB clock (F_{SSPCLK}).

[3)] Slave-Mode : SCLK_IN is synchronized in (2 internal clocks)

Note

Operation without SPI_FRAME_N:

If the ERTEC 200P-3 is connected as SPI slave to a standard controller (SPI master) that does not support the SPI_FRAME_N signal, the ERTEC 200P-3 is to be set as follows:

- Configuration of Motorola format: SSPCR0.FRF = '00') AND
- Configuration of the SPI clock phase: SSPCR0.SPH = '1' AND
- GPIO pin SPI_FRAME_N (see chaper 2.2)
  - Connect with ext. Pull-down OR
  - Connect with int. Pull-down (PULLxx_yyGPIO = "11" OR
  - Do not select the alternate function (blocking value = '0' is active)

Please not the following restrictions in this operating mode:

In the SPI status register, SSPSR.BSY is not reset at the end of the transfer. Following a RESET, "zero data" is transferred when the first character (4-bit...16-bit, SSPCR0.DSS) is transferred from the SPI slave to the SPI master (return direction).

2.3.6 UART Timing

Table 2-30: UART1 Timing (1.8 V)

Signal	Output Runtime (ns)		Input Runtime (ns)	
	$T_{OR\ min}$	$T_{OR\ max}$	$T_{IR\ min}$	$T_{IR\ max}$
XHIF_A17 (U1_CTS)			2.7	8.5
XHIF_A18 (U1_DCD)			2.5	8.5
XHIF_A19 (U1_DSR)			2.5	8.4
XHIF_SEG_2 (U1_RI)			2.5	8.5
XHIF_SEG_0 (U1_RTS)	3.5	12.2		
XHIF_SEG_1 (U1_DTR)	3.3	12.3		
XHIF_XBE2 (U1_TXD)	3.6	12.8		
XHIF_XBE3 (U1_RXD)			2.8	9.5
Based on	Buffer Drive strength = 8 mA, pin load 20 pf IO-Voltage = 1.8 V			

Table 2-31: UART1 Timing (3.3 V)

Signal	Output Runtime (ns)		Input Runtime (ns)	
	$T_{OR\ min}$	$T_{OR\ max}$	$T_{IR\ min}$	$T_{IR\ max}$
XHIF_A17 (U1_CTS)			2.5	8.1
XHIF_A18 (C) (U1_DCD)			2.3	8.1
XHIF_A19 (U1_DSR)			2.3	8.0
XHIF_SEG_2 (U1_RI)			2.3	8.0
XHIF_SEG_0 (U1_RTS)	2.7	7.0		
XHIF_SEG_1 (U1_DTR)	2.6	7.1		
XHIF_XBE2 (U1_TXD)	2.9	7.6		
XHIF_XBE3 (U1_RXD)			2.6	9.1
Based on	Buffer Drive strength = 8 mA, pin load 20 pf IO-Voltage = 3.3 V			

Table 2-32: UART2 Timing

Signal	Output Runtime (ns)		Input Runtime (ns)	
	$T_{OR\ min}$	$T_{OR\ max}$	$T_{IR\ min}$	$T_{IR\ max}$
GPIO12_INT(B) (U2_CTS)			1.8	5.2
GPIO13_INT(B) (U2_RTS)	3.2	8.7		
GPIO14_INT(B) (U2_TXD)	3.2	8.4		
GPIO15_INT(B) (U2_RXD)			2.1	6.3
Based on	Buffer Drive strength = 8 mA, pin load 20 pf IO-Voltage = 3.3 V			

Table 2-33: UART3 Timing

Signal	Output Runtime (ns)		Input Runtime (ns)	
	$T_{OR\ min}$	$T_{OR\ max}$	$T_{IR\ min}$	$T_{IR\ max}$
GPIO28(B) (U3_TXD)	3.1	8.4		
GPIO29(B) (U3_RXD)			1.8	5.6
Based on	Buffer Drive strength = 8 mA, pin load 20 pf IO-Voltage = 3.3 V			

Table 2-34: UART4 Timing (1.8 V)

Signal	Output Runtime (ns)		Input Runtime (ns)	
	$T_{OR\ min}$	$T_{OR\ max}$	$T_{IR\ min}$	$T_{IR\ max}$
XHIF_XRDY (U4_TXD)	3.5	12.2		
XHIF_IRQ (U4_RXD)			2.5	7.5
Based on	Buffer Drive strength = 8 mA, pin load 20 pf IO-Voltage = 1.8 V			

Table 2-35: UART4 Timing (3.3 V)

Signal	Output Runtime (ns)		Input Runtime (ns)	
	$T_{OR\ min}$	$T_{OR\ max}$	$T_{IR\ min}$	$T_{IR\ max}$
XHIF_XRDY (U4_TXD)	2.7	7.1		
XHIF_IRQ (U4_RXD)			2.3	7.0
Based on	Buffer Drive strength = 8 mA, pin load 20 pf IO-Voltage = 3.3 V			

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2.3.7 I²C Timing

2.3.7.1 I²C – APB

Table 2-36: I²C - APB Timing

Symbol	Port	Parameter	Min.	Max.	Unit	Note
$T_{out\ SCLK}$	GPIO14_INT	SCLK Output delay	2.5	9.7	ns	
$T_{out\ SDIO}$	GPIO15_INT	SDIO Output delay	2.5	10.2	ns	
$T_{in\ SCLK}$	GPIO14_INT	SCLK Input delay	2.1	7.2	ns	
$T_{in\ SDIO}$	GPIO15_INT	SDIO Input delay	2.1	7.1	ns	
Based on		Buffer Drive strength = 8 mA, pin load 20 pf IO-Voltage = 3.3 V				

Table 2-37: I²C - APB Timing Alternative 1

Symbol	Port	Parameter	Min.	Max.	Unit	Note
$T_{out\ SCLK}$	GPIO30	SCLK Output delay	1.9	8.4	ns	
$T_{out\ SDIO}$	GPIO31	SDIO Output delay	2.0	8.7	ns	
$T_{in\ SCLK}$	GPIO30	SCLK Input delay	1.9	7.6	ns	
$T_{in\ SDIO}$	GPIO31	SDIO Input delay	1.9	7.5	ns	
Based on		Buffer Drive strength = 8 mA, pin load 20 pf IO-Voltage = 3.3 V				

Table 2-38: I²C - APB Timing Alternative 2 (1.8 V)

Symbol	Port	Parameter	Min.	Max.	Unit	Note
$T_{out\ SCLK}$	XHIF_A16	SCLK Output delay	2.1	13.3	ns	
$T_{out\ SDIO}$	XHIF_A17	SDIO Output delay	2.3	14.0	ns	
$T_{in\ SCLK}$	XHIF_A16	SCLK Input delay	2.1	7.4	ns	
$T_{in\ SDIO}$	XHIF_A17	SDIO Input delay	2.0	7.1	ns	
Based on		Buffer Drive strength = 8 mA, pin load 20 pf IO-Voltage = 1.8 V				

Table 2-39: I²C - APB Timing Alternative 2 (3.3 V)

Symbol	Port	Parameter	Min.	Max.	Unit	Note
$T_{out\ SCLK}$	XHIF_A16	SCLK Output delay	1.8	8.1	ns	
$T_{out\ SDIO}$	XHIF_A17	SDIO Output delay	2.0	8.7	ns	
$T_{in\ SCLK}$	XHIF_A16	SCLK Input delay	1.9	6.9	ns	
$T_{in\ SDIO}$	XHIF_A17	SDIO Input delay	1.8	6.6	ns	

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Based on		Buffer Drive strength = 8 mA, pin load 20 pf IO-Voltage = 3.3 V

2.3.7.2 I²C – PN-IP

Table 2-40: I²C - PN-IP Timing

Symbol	Port	Parameter	Min.	Max.	Unit	Note
$T_{out\ SCLK}$	GPIO5_INT	SCLK Output delay	2.8	11.6	ns	
$T_{out\ SDIO}$	GPIO4_INT	SDIO Output delay	3.1	11.7	ns	
$T_{in\ SCLK}$	GPIO5_INT	SCLK Input delay	3.2	11.4	ns	
$T_{in\ SDIO}$	GPIO4_INT	SDIO Input delay	3.0	11.0	ns	
Based on		Buffer Drive strength = 8 mA, pin load 20 pf IO-Voltage = 3.3 V				

Table 2-41: I²C - PN-IP Timing Alternative 1

Symbol	Port	Parameter	Min.	Max.	Unit	Note
$T_{out\ SCLK}$	GPIO7_INT	SCLK Output delay	3.0	11.2	ns	
$T_{out\ SDIO}$	GPIO6_INT	SDIO Output delay	3.1	11.6	ns	
$T_{in\ SCLK}$	GPIO7_INT	SCLK Input delay	3.1	11.3	ns	
$T_{in\ SDIO}$	GPIO6_INT	SDIO Input delay	3.4	12.3	ns	
Based on		Buffer Drive strength = 8 mA, pin load 20 pf IO-Voltage = 3.3 V				

Table 2-42: I²C - PN-IP Timing Alternative 2 (1.8 V)

Symbol	Port	Parameter	Min.	Max.	Unit	Note
$T_{out\ SCLK}$	XHIF_D17	SCLK Output delay	3.2	16.1	ns	
$T_{out\ SDIO}$	XHIF_D16	SDIO Output delay	3.3	16.2	ns	
$T_{in\ SCLK}$	XHIF_D17	SCLK Input delay	3.8	12.7	ns	
$T_{in\ SDIO}$	XHIF_D16	SDIO Input delay	3.6	12.8	ns	
Based on		Buffer Drive strength = 8 mA, pin load 20 pf IO-Voltage = 1.8 V				

Table 2-43: I²C - PN-IP Timing Alternative 2 (3.3 V)

Symbol	Port	Parameter	Min.	Max.	Unit	Note
$T_{out\ SCLK}$	XHIF_D17	SCLK Output delay	2.9	10.8	ns	
$T_{out\ SDIO}$	XHIF_D16	SDIO Output delay	3.1	11.0	ns	
$T_{in\ SCLK}$	XHIF_D17	SCLK Input delay	3.6	12.3	ns	

$T_{in\ SDIO}$	XHIF_D16	SDIO Input delay	3.4	12.3	ns	
Based on		Buffer Drive strength = 8 mA, pin load 20 pf IO-Voltage = 3.3 V				

Table 2-44: I²C - PN-IP Timing Alternative 3 (1.8 V)

Symbol	Port	Parameter	Min.	Max.	Unit	Note
$T_{out\ SCLK}$	XHIF_D19	SCLK Output delay	3.0	15.7	ns	
$T_{out\ SDIO}$	XHIF_D18	SDIO Output delay	3.1	15.9	ns	
$T_{in\ SCLK}$	XHIF_D19	SCLK Input delay	3.8	13.2	ns	
$T_{in\ SDIO}$	XHIF_D18	SDIO Input delay	3.8	13.5	ns	
Based on		Buffer Drive strength = 8 mA, pin load 20 pf IO-Voltage = 1.8 V				

Table 2-45: I²C - PN-IP Timing Alternative 3 (3.3 V)

Symbol	Port	Parameter	Min.	Max.	Unit	Note
$T_{out\ SCLK}$	XHIF_D19	SCLK Output delay	2.7	10.4	ns	
$T_{out\ SDIO}$	XHIF_D18	SDIO Output delay	2.9	10.6	ns	
$T_{in\ SCLK}$	XHIF_D19	SCLK Input delay	3.6	12.8	ns	
$T_{in\ SDIO}$	XHIF_D18	SDIO Input delay	3.6	13.1	ns	
Based on		Buffer Drive strength = 8 mA, pin load 20 pf IO-Voltage = 3.3 V				

2.3.8 GPIO Timing

The GPIO interface is asynchronous to external signals. External inputs will be synchronized internally.

All inputs have no timing relation from an external clock to internal clock of ERTEC 200P.

All outputs have no timing relation from internal clock of ERTEC 200P-3 to an external clock.

Table 2-46: GPIO Timing

Symbol	Description	Min	Max	Unit	Note
T_{din}	Runtime of Input signals	1.2	9.2	ns	1)
T_{dout}	Runtime of Output signals	2.1	9.7	ns	1)
$T_{din\ skew}$	Skew of Input signals	-	7.1	ns	1)
$T_{dout\ skew}$	Skew of Output signals	-	5.3	ns	1)
Based on	Buffer Drive strength = 8mA IO-Voltage = 3.3 V				

1) C_L = 20 pF

2.3.9 JTAG Timing

The JTAG interface consists of the TCK, TMS, TDI, TDO, and TRST signals. All input signals except TRST are clocked in with a TCK rising edge. The TDO signal is output with a TCK falling edge.

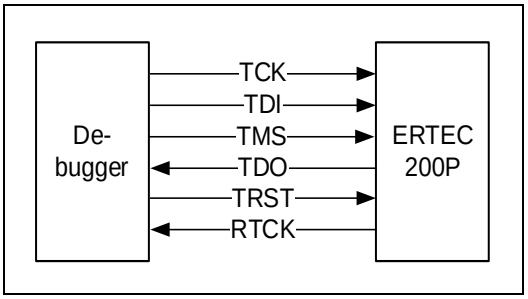

Figure 2-13: Debug interface

The JTAG clock is to be operated up to a frequency of 32 MHz (RTCK evaluation in the debugger). A minimum hold time of 0 ns shall be used for the inputs of the debug interface. Only a JTAG clock of up to 16 MHz can be used for debuggers that do not support RTCK.

2.3.10 OctalSPI Timing

Values required by the memories must correspond to the values provided by the ASIC and vice versa.

Table 2-47: OctalSPI Timing (3.3 V at 15 pF load)

Symbol	**Parameter (**output: ASIC → memory)	**Min.**	**Max.**	**Unit**	**Note**
T_{DVCH}	D setup time to clock rise	3.7	-	ns	1)
T_{DVCL}	D setup time to clock fall	3.7	-	ns	1)
T_{CHDX}	D hold time from clock rise	2.7	-	ns	1)
T_{CLDX}	D hold time from clock fall	2.7	-	ns	1)
T_{SLCH}	CS active setup time to clock rise	12.7	-	ns	1)
T_{CHSH}	CS active hold time after clock rise	7.3	-	ns	1)
T_{CLSH}	CS active hold time after clock fall	7.3	-	ns	1)
Symbol	**Parameter** (input: memory → ASIC)	**Min.**	**Max.**	**Unit**	**Note**
	mode: without RXDS				
T_{CLQV}	DQ valid after clock fall	-	10.5	ns	2)
T_{CHQV}	DQ valid after clock rise	-	10.3	ns	2)
T_{CLQX}	DQ invalid after clock fall	8.8	-	ns	3)
T_{CHQX}	DQ invalid after clock rise	8.8	-	ns	3)
	mode: internal RXDS				
T_{CLQV_rxds}	DQ valid after clock fall – internal RXDS	-	5.3	ns	2), 4)
T_{CHQV_rxds}	DQ valid after clock rise – internal RXDS	-	5.3	ns	2), 4)
T_{CLQX_rxds}	DQ invalid after clock fall – internal RXDS	1.2	-	ns	3), 4)
T_{CHQX_rxds}	DQ invalid after clock rise – internal RXDS	1.2	-	ns	3), 4)
	mode: external RXDS				
T_{DQSQ}	DQS to DQ valid	-	1.3	ns	2)
T_{DVW}	Data Valid Window	3.5	-	ns	3)
Based on	Buffer driver strength = 8 mA, pin load 15 pf, DDR with 62.5 MHz clock frequency				

1) Value provided by ERTEC, value required by memory/board must be smaller

2) Value required by ERTEC, value provided by memory/board must be smaller

3) Value required by ERTEC, value provided by memory/board must be larger

4) Internally generated RXDS can be shifted with a resolution of 1.0 ns.
These values change accordingly in steps of 1.0 ns (e.g., 5.3 ns → 6.3 ns, 1.2 ns → 2.2 ns)

Note

Concerning mode “without RXDS”:
This mode will not work with DDR at maximum SCLK frequency of 62.5 MHz. With SDR (or with 31.25 MHz) CLQX/CHQX improve by 8 ns.

Note that in this mode, the IP’s internal sampling time can be shifted by multiples of 8 ns by parameterization.
The HWAL will take care of this. Default setting for the values above is a shift by 24 ns.

Concerning mode “internal RXDS”:
In this mode, the IP’s internal sampling time can be shifted by multiples of 1 ns by parameterization. The HWAL will take care of this. Default setting for the values above is a shift by 4 ns.

Table 2-48: OctalSPI Timing (1.8 V at 15 pF load)

Symbol	Parameter (output: ASIC → memory)	Min.	Max.	Unit	Note
T_{DVCH}	D setup time to clock rise	3.8	-	ns	1)
T_{DVCL}	D setup time to clock fall	3.3	-	ns	1)
T_{CHDX}	D hold time from clock rise	2.3	-	ns	1)
T_{CLDX}	D hold time from clock fall	3.1	-	ns	1)
T_{SLCH}	CS active setup time to clock rise	12.1	-	ns	1)
T_{CHSH}	CS active hold time after clock rise	7.5	-	ns	1)
T_{CLSH}	CS active hold time after clock fall	8.2	-	ns	1)
Symbol	**Parameter** (input: memory → ASIC)	**Min.**	**Max.**	**Unit**	**Note**
	mode: without RXDS				
T_{CLQV}	DQ valid after clock fall	-	6.9	ns	2)
T_{CHQV}	DQ valid after clock rise	-	5.9	ns	2)
T_{CLQX}	DQ invalid after clock fall	7.9	-	ns	3)
T_{CHQX}	DQ invalid after clock rise	7.6	-	ns	3)
	mode: internal RXDS				
T_{CLQV_rxds}	DQ valid after clock fall	-	5.2	ns	2), 4)
T_{CHQV_rxds}	DQ valid after clock rise	-	5.2	ns	2), 4)
T_{CLQX_rxds}	DQ invalid after clock fall	0.9	-	ns	3), 4)
T_{CHQX_rxds}	DQ invalid after clock rise	0.9	-	ns	3), 4)
	mode: external RXDS				
T_{DQSQ}	DQS to DQ valid	-	1.7	ns	2)
T_{DVW}	Data Valid Window	3.5	-	ns	3)
Based on	Buffer driver strength = 4 mA, pin load 15 pf, DDR with 62.5 MHz clock frequency				

1) Value provided by ERTEC, value required by memory/board must be smaller

2) Value required by ERTEC, value provided by memory/board must be smaller

3) Value required by ERTEC, value provided by memory/board must be larger

4) Internally generated RXDS can be shifted with a resolution of 1.0 ns.
These values change accordingly in steps of 1.0 ns (e.g., 5.2 ns → 6.2 ns, 0.9ns → 1.9 ns)

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Note

Concerning mode “without RXDS”:
This mode will not work with DDR at maximum SCLK frequency of 62.5 MHz. With SDR (or with 31.25 MHz) CLQX/CHQX improve by 8 ns.
Note that in this mode, the IP’s internal sampling time can be shifted by multiples of 8 ns by parameterization.
The HWAL will take care of this. Default setting for the values above is a shift by 24 ns.

Concerning mode “internal RXDS”:
In this mode, the IP’s internal sampling time can be shifted by multiples of 1 ns by parameterization.
The HWAL will take care of this. Default setting for the values above is a shift by 5 ns.

Table 2-49: OctalSPI Timing (3.3 V at 10 pF load)

Symbol	**Parameter (**output: ASIC → memory)	**Min.**	**Max.**	**Unit**	**Note**
T_{DVCH}	D setup time to clock rise	3.7	-	ns	1)
T_{DVCL}	D setup time to clock fall	3.7	-	ns	1)
T_{CHDX}	D hold time from clock rise	2.7	-	ns	1)
T_{CLDX}	D hold time from clock fall	2.8	-	ns	1)
T_{SLCH}	CS active setup time to clock rise	12.3	-	ns	1)
T_{CHSH}	CS active hold time after clock rise	7.1	-	ns	1)
T_{CLSH}	CS active hold time after clock fall	7.2	-	ns	1)
Symbol	**Parameter** (input: memory → ASIC)	**Min.**	**Max.**	**Unit**	**Note**
	mode: without RXDS				
T_{CLQV}	DQ valid after clock fall	-	10.8	ns	2)
T_{CHQV}	DQ valid after clock rise	-	10.6	ns	2)
T_{CLQX}	DQ invalid after clock fall	8.9	-	ns	3)
T_{CHQX}	DQ invalid after clock rise	8.9	-	ns	3)
	mode: internal RXDS				
T_{CLQV_rxds}	DQ valid after clock fall – internal RXDS	-	5.3	ns	2), 4)
T_{CHQV_rxds}	DQ valid after clock rise – internal RXDS	-	5.3	ns	2), 4)
T_{CLQX_rxds}	DQ invalid after clock fall – internal RXDS	1.2	-	ns	3), 4)
T_{CHQX_rxds}	DQ invalid after clock rise – internal RXDS	1.2	-	ns	3), 4)
	mode: external RXDS				
T_{DQSQ}	DQS to DQ valid	-	1.3	ns	2)
T_{DVW}	Data Valid Window	3.5	-	ns	3)
Based on	Buffer driver strength = 8 mA, pin load 10 pf, DDR with 62.5 MHz clock frequency				

1) Value provided by ERTEC, value required by memory/board must be smaller

2) Value required by ERTEC, value provided by memory/board must be smaller

3) Value required by ERTEC, value provided by memory/board must be larger

4) Internally generated RXDS can be shifted with a resolution of 1.0 ns.
These values change accordingly in steps of 1.0 ns (e.g., 5.3 ns → 6.3 ns, 1.2ns → 2.2 ns)

Note

Concerning mode “without RXDS”:
This mode will not work with DDR at maximum SCLK frequency of 62.5 MHz. With SDR (or with 31.25 MHz) CLQX/CHQX improve by 8 ns.
Note that in this mode, the IP’s internal sampling time can be shifted by multiples of 8 ns by parameterization.
The HWAL will take care of this. Default setting for the values above is a shift by 24 ns.

Concerning mode “internal RXDS”:
In this mode, the IP’s internal sampling time can be shifted by multiples of 1 ns by parameterization.
The HWAL will take care of this. Default setting for the values above is a shift by 4 ns.

Table 2-50: OctalSPI Timing (1.8 V at 10 pF load)

Symbol	Parameter (output: ASIC → memory)	Min.	Max.	Unit	Note
T_{DVCH}	D setup time to clock rise	3.8	-	ns	1)
T_{DVCL}	D setup time to clock fall	3.3	-	ns	1)
T_{CHDX}	D hold time from clock rise	2.3	-	ns	1)
T_{CLDX}	D hold time from clock fall	3.1	-	ns	1)
T_{SLCH}	CS active setup time to clock rise	12.1	-	ns	1)
T_{CHSH}	CS active hold time after clock rise	7.5	-	ns	1)
T_{CLSH}	CS active hold time after clock fall	8.2	-	ns	1)
Symbol	**Parameter** (input: memory → ASIC)	**Min.**	**Max.**	**Unit**	**Note**
	mode: without RXDS				
T_{CLQV}	DQ valid after clock fall	-	6.9	ns	2)
T_{CHQV}	DQ valid after clock rise	-	5.9	ns	2)
T_{CLQX}	DQ invalid after clock fall	7.9	-	ns	3)
T_{CHQX}	DQ invalid after clock rise	7.6	-	ns	3)
	mode: internal RXDS				
T_{CLQV_rxds}	DQ valid after clock fall	-	5.2	ns	2), 4)
T_{CHQV_rxds}	DQ valid after clock rise	-	5.2	ns	2), 4)
T_{CLQX_rxds}	DQ invalid after clock fall	0.9	-	ns	3), 4)
T_{CHQX_rxds}	DQ invalid after clock rise	0.9	-	ns	3), 4)
	mode: external RXDS				
T_{DQSQ}	DQS to DQ valid	-	1.7	ns	2)
T_{DVW}	Data Valid Window	3.5	-	ns	3)
Based on	Buffer driver strength = 4 mA, pin load 10 pF, DDR with 62.5 MHz clock frequency				

1) Value provided by ERTEC, value required by memory/board must be smaller

2) Value required by ERTEC, value provided by memory/board must be smaller

3) Value required by ERTEC, value provided by memory/board must be larger

4) Internally generated RXDS can be shifted with a resolution of 1.0 ns.
These values change accordingly in steps of 1.0 ns (e.g., 5.2 ns → 6.2 ns, 0.9 ns → 1.9 ns)

Note

Concerning mode “without RXDS”:
This mode will not work with DDR at maximum SCLK frequency of 62.5 MHz. With SDR (or with 31.25 MHz) CLQX/CHQX improve by 8 ns.
Note that in this mode, the IP’s internal sampling time can be shifted by multiples of 8 ns by parameterization.
The HWAL will take care of this. Default setting for the values above is a shift by 24 ns.

Concerning mode “internal RXDS”:
In this mode, the IP’s internal sampling time can be shifted by multiples of 1 ns by parameterization.
The HWAL will take care of this. Default setting for the values above is a shift by 5 ns.

3 Layout and Design Hints

3.1 Analog PLL

PLL_A (Module PLLTS40LPFRAC from Silicon Creation)

- Input Clock: 25 MHz
- Output Clock: 500 MHz (FBDV = 20, equals f_{VCO})
- Integer Mode (DSMPD = '1')
- PD (pll_b_stby) should be activated for at least 1 µs at power-up (covered by Lock Timer1)
- t_{Lock} = 60 µs (covered by Lock Timer2)
- Period Jitter = 467 fs

The main focus has to be set on the stability of the output clock-signal. For the whole line of resonator, oscillator and PLL the following accuracy is needed: **< ± 100ps period jitter**

Tabelle 3-1: PLL Wiring

Signal	Type	Function	
BYPASS	IN	FREF is bypassed to FOUTPOSTDIV	0
CLKSSCG	OUT	Synchronization clock for spread spectrum modulation	open
DACPD	IN	Power down noise canceling DAC in FRAC mode	0
DSMPD	IN	Power down Delta-Sigma Modulator	1
FBDIV[11:0]	IN	PLL Feedback divide value	20
FOUT1PH0	OUT	Auxiliary 4 phase output at 0°	open
FOUT1PH180	OUT	Auxiliary 4 phase output at 180°	open
FOUT1PH270	OUT	Auxiliary 4 phase output at 270°	open
FOUT1PH90	OUT	Auxiliary 4 phase output at 90°	open
FOUT2	OUT	PLL auxiliary output (div 2)	open
FOUT3	OUT	PLL auxiliary output (div 6)	open
FOUT4	OUT	PLL auxiliary output (div 8)	open
FOUT4PHASEPD	IN	Power down of 4 phase clock generator	1
FOUTPOSTDIV	OUT	PLL post divided output	open
FOUTPOSTDIVPD	IN	Post divided power down	1
FOUTVCO	OUT	VCO rate output clock	clk_pll
FOUTVCOPD	IN	VCO rate output clock power down	0
FRAC[23:0]	IN	Fractional portion of feedback divide value	0

Signal	Type	Function	
FREF	IN	Reference clock input	CLK_A_CTS
LOCK	OUT	Lock signal	open
PD	IN	Power Down for PLL	pll_a_stby
POSTDIV1[2:0]	IN	PLL post divide 1	1
POSTDIV2[2:0]	IN	PLL post divide 2	1
REFDIV[5:0]	IN	Reference divide value	1

3.2 EMC Measures

3.2.1 ESD Protection

ESD robustness

- Human Body Model (HBM) 1000 V
- Charge Device Model (CDM) 500 V

3.2.2 Immunity to ESD

The ERTEC 200P-3 ASIC and the systems/devices fitted with it are designed for EMC in accordance with [EN] IEC 61000-6-2 (Electromagnetic compatibility - Generic standards - Immunity for industrial environments) and [EN] IEC 61000-6-4 (Electromagnetic compatibility - Generic standards - Emission standard for industrial environments).

These standards are the device standards for use in industrial environments. For compliance with these device standards, however, the EMC of the individual integrated circuits used (in particular immunity to interference in operation) is decisive.

To ensure an ASIC is as immune as possible, great care must be taken in the design, the layout and the selection of IO cell characteristics to ensure immunity to interference in operation and to minimize emission.

3.2.3 Spike Filter

The same spike filters are implemented for the test inputs TAP_SEL and TACT at the input as for the reset inputs (XRESET, XSRST, XTRST) and for CHAIN_CTRL. The filters ensure that spikes <= 60 ns (best case) are suppressed. This ensures a time constant of 60 ns between the pin and function (low-pass).

Note

A spike at TAP_SEL, XTRST and/or TACT is not forwarded to the JTAG controller as this would require a sequence over TDI/TMS and TCK from the debugger.

The ERTEC 200P-3 does contain a spike filter of 60 ns (best case condition) for following signals:

- XRESET (Reset)
- XSRST (Debugger Reset)
- XTRST (JTAG Reset)
- TAP_SEL (TAP Select)
- CHAIN_CTRL (Multicore Debugging)
- TACT (Testmode)

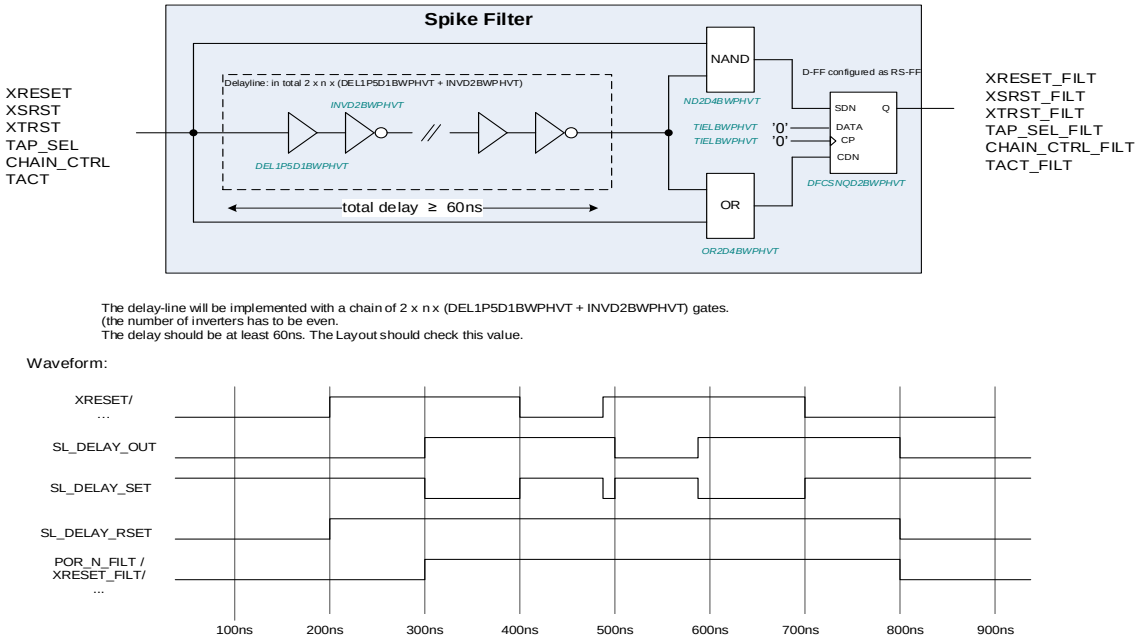

Figure 3-1: Spike Filter Implementation

To ensure the XRESET-, XSRST-, XTRST-, TAP_SEL-, CHAIN_CTRL- and TACT-signals will not be blocked by the spike filter, the pulse width must be wider than 220 ns.

3.3 Crystal Oscillator Layout

ERTEC 200P-3 requires a 25 MHz clock source. There are 3 use cases to supply this clock:

- Use case 1: External crystal and internal oscillator
- Use case 2: External oscillator cell / CMOS clock input
- Use case 3: External MEMS oscillator

2 Pins/Balls are used to realize the clock supply:

- Input XTAL1
- Output XTAL2

3.3.1 Use case 1: External crystal, internal oscillator

Figure 3-2 shows the required circuit to connect a crystal to the ERTEC 200P-3.

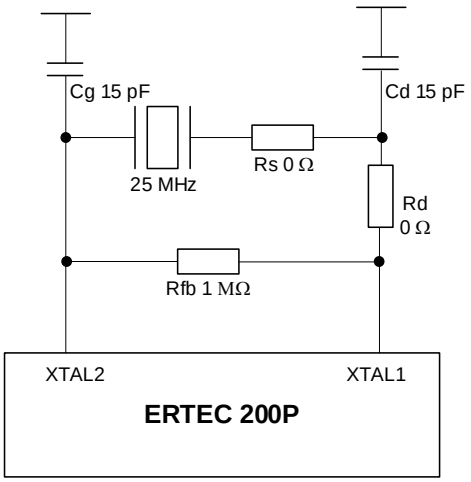

Figure 3-2: Oscillator Circuitry[1]

Rd is optional to reduce the driver level seen by the crystal and Rs can be used to determine the safety factor of the oscillator circuit.

The values of Cg and Cd depend on the chosen crystal CL and ERTEC IO pin capacity.

Pin input/ output capacity (incl. package):

Parameter	Signal/ Description	In/Out	Pin	Value
C_{in}	XTAL1	Input	A9	1.80 pF
C_{out}	XTAL2	Output	B9	2.24 pF

[1] For fast startup applications it is required to use an external clock source.

The following oscillator crystals are recommended:

- TSX-3225/ NX2520SA
  - Epson: X 1E000021 013800
  - NDK: EXS00A-CS13406

Parameter	Description	Value
F	Nominal (fundamental) Frequency	25 MHz
Order	Overtone Order	Fundamental
ESR_{max}	Maximum Equivalent Series Resistor	≤40 Ω
C_L	Load Capacitance	10 pF
DL_{max}	Maximum Drive Level	≤200 µW
$F_{Tolerance}$	Frequency Tolerance	40 ppm (@20 years)
$T_{Operation}$	Operating Temperature	-40°C to +85°C

Equivalent crystal model:

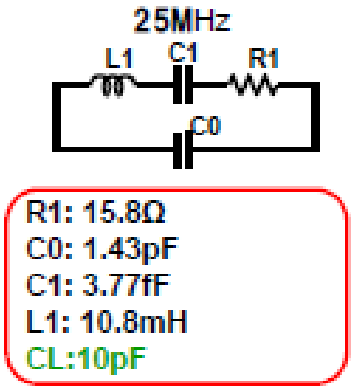

Figure 3-3: Equivalent Crystal Model

Note

The oscillator frequency must be 25 MHz, otherwise the PLL will not operate properly.

If a different crystal is used the following conditions must be met:

- Crystal with 25MHz with a maximum of ± 50ppm over the whole lifetime and temperature range.
- The values for Rd, C_{in}, C_{out} must be calculated accordingly.
- To meet the FSU (fast startup) requirement, the quartz startup time must be < 20 ms

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PCB layout hints:

- Place the input and output pins of the oscillator and the resonator and external components close to each other and keep wiring as short as possible.
- Use a wiring as short and as thick as possible between the ground side of the capacitor and the ground pin of the ERTEC 200P.
- Keep the lead wire of the resonator and capacitor as short as possible and fix the resonator and capacitor to the printed circuit board to keep the influence of mechanical vibrations to a minimum.
- If possible, arrange the external constant portion so that it is surrounded by GND.

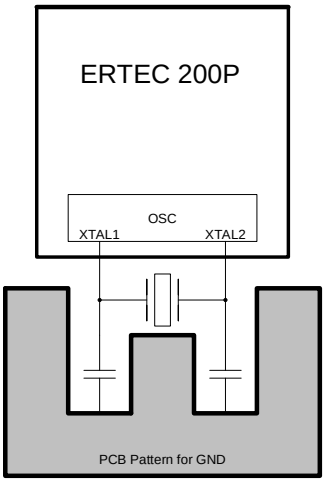

Figure 3-4: Oscillator Circuitry Layout Example

Note

For every PCB design the measurements for the startup time of the oscillator must be done with the above circuit. If necessary, the dimensioning of the circuit or the startup of the device must be adapted (extension of reset duration).

3.3.2 Use case 2: External oscillator cell / CMOS clock input

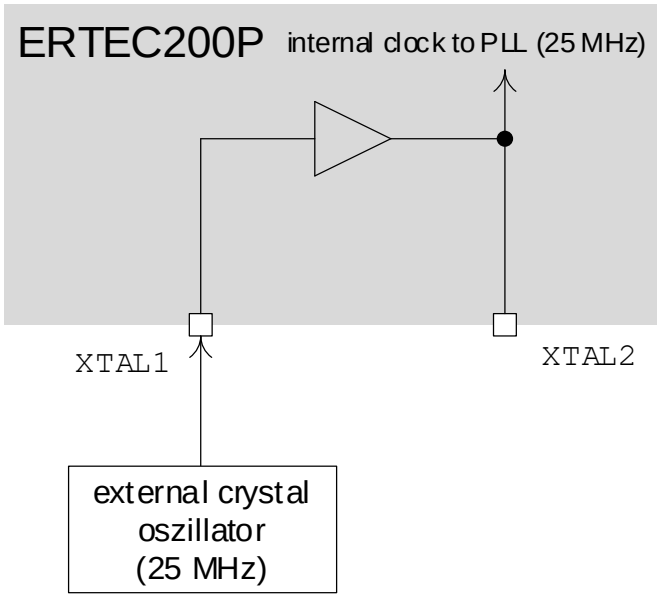

Figure 3-5: External Oscillator

The usage of an external oscillator is supported. The external oscillator is connected to XTAL1. XTAL2 can be left open.

3.3.3 Use case 3: External MEMS oscillator

MEMS oscillators with the following data (or better) can be used:

Parameter	Description	Range / Value
F	Nominal Frequency	25 MHz
$F_{Tolerance}$	Frequency Tolerance	+/-50 ppm (@20 years)
$T_{Operation}$	Operating Temperature	-40 °C to +105 °C
T_{jitt}	Root Mean Square Period Jitter	5 ps (f = 25 MHz, Vdd = 3.3V)
T_{pk}	Peak-to-peak Period Jitter	30 ps (f = 25 MHz, Vdd = 3.3V)
T_{phj}	Root Mean Square Phase Jitter (random)	2 ps (f = 25 MHz, small integration bandwidth)

3.4 Test Signal Configuration

Table 3-1: Test Signal Configuration

Test Pins	External Wiring in Function Mode	Internal Wiring
TEST	low-impedance to ground (GND)	- Pull-down (ca. 50kΩ) **- no** spike filter!
TACT	low-impedance to ground (GND)	- Pull-down (ca. 50kΩ) - spike filter < 60 ns
TAP_SEL	low-impedance to ground (GND)	- **no** pull! - spike filter < 60 ns
TMC1	straight to ground (GND)	- Pull-down (ca. 50kΩ) **- no** spike filter!
TMC2	straight to ground (GND)	- Pull-down (ca. 50kΩ) **- no** spike filter!

The module design must comply **strictly** with the external test signal configuration given in the table.

For the module test, the ERTEC 200P-3 can be switched to boundary scan mode by setting the test signals as shown in the following table:

TACT	TAP_SEL	TEST	TMC1	TMC2	Description
0	0	0	0	0	Function mode
1	1	0	0	0	ERTEC 200P-3 boundary scan mode

The boundary scan is controlled over the JTAG interface (see 2.3.9).

3.5 JTAG Wiring

The JTAG interface is an interface over which the boundary scan register can be controlled or which can be used for ERTEC 200P-3 debugging. The JTAG reset is purposefully implemented without an internal pull resistor so that various debugger connections are possible. A filter integrated in ERTEC 200P-3 ensures that spikes <= 60 ns (best case) at JTAG reset XTRST are suppressed (see 3.2.3).

The table below shows the various recommendations for external Pull-up/down configurations of the JTAG interface signals.

JTAG Signal	**Signal Direction**	**ERTEC 200P -3 internal pull** (see chapter. 2.2)	**Circuit for Production** (ETB not accessible via AHB)	**Circuit for Debugging, ARM recommended** (ETB accessible via AHB)	**recommended JTAG circuit**	**Recommendation from Debug supplier (Lauterbach[1])**
XTRST	in	Pull-down	**10k Pull-down**	4k7 Pull-up	10k Pull-down default and 4k7 Pull-up Assembly option	You shall place a Pull-down resistor (1k - 47k) on this signal on target side, although this is not JTAG conform. It ensures the on-chip debug logic is inactive when the debugger is not connected. Pull-down ==> Production Pull-up ==> Debugging
RTCK	in/out	-	*not necessary*	4k7 Pull-down	4k7 Pull-down	If this is not required, then it can be used to compensate the propagation delays on driver and cable. This allows to reach higher JTAG clock frequencies. Therefore you need to feed-back the TCK signal buffered or unbuffered to this line. On an unbuffered feed-back it might have negative effect on signal reflection. Better provide a chance to cut the connection on the target (jumper or solder bridge) in case problems arise.
TCK	In	Pull-down	*not necessary*	4k7 Pull-down	4k7 Pull-down	You shall place a Pull-up or Pull-down resistor (1k - 47k) on this line in order to give it a defined state even when the line is not driven by the debugger.
TDI	In	Pull-up	*not necessary*	4k7 Pull-up	4k7 Pull-up	You can place a Pull-up or Pull-down resistor (1k - 47k) on this line to ensure a defined state even when the line is not driven by the debugger.
TMS	In	Pull-up	*not necessary*	4k7 Pull-up	4k7 Pull-up	You can place a Pull-up or Pull-down resistor (1k - 47k) on this line in order to give it a defined state even when the line is not driven by the debugger.
XSRST	In	Pull-up	*not necessary because of internal Pull-up*	*not necessary, because of internal Pull-up*	*not necessary, because internal Pull-up*	There might be the need to place a Pull-up (1k - 47k) on target side to avoid unintentional resets when the debugger is not connected and probably to strengthen the weak 47k Pull-up in the debug cable.
TDO	out	-	*not necessary*	*not necessary*	33Ω series resistor	You can place a 33 series resistor close to the processor for series termination. You can place a Pull-up or Pull-down resistor (1k - 47k) on this

[1] See document “ARM JTAG Interface Specification” from Lauterbach

JTAG Signal	Signal Direction	ERTEC 200P-3 internal pull (see chapter. 2.2)	Circuit for Production (ETB not accessible via AHB)	Circuit for Debugging, ARM recommended (ETB accessible via AHB)	recommended JTAG circuit	Recommendation from Debug supplier (Lauterbach[1])
						line.

Note

To achieve the best possible resistance to interference on the module (see "Circuit for Production" column in the table above), the XTRST pin on the module must have a 10 KΩ Pull-down. This deactivates JTAG interface during operation, which means that noise pulses affecting the individual JTAG signals can no longer affect ERTEC 200P-3 function. If a debugger is used at the JTAG interface, the Pull-down has no effect as the debugger actively pulls the XTRST signal to '1'. Only AHB access to the ETM trace buffer SRAM is not possible in this configuration. If access from an AHB master (e.g. ARM926) to this SRAM (ETB) is required for test purposes, the XTRST pin requires a 10 KΩ Pull-up. Please note that AHB access to the ETM trace buffer SRAM is only possible in this case if no debugger is connected.

3.5.1 JTAG ID

The JTAG target ID (for debugging) of ERTEC 200P-3 is 0x022F0031. This is based on the specification from the vendor and is to be interpreted as follows:

Siemens-specific				Vendor-specific (ID-Code = 0x18, Continuation Code = 0)			
[31:28]	[27:24]	[23:16]	[15:12]	[11:8]	[7:5]	[4:1]	[0]
Revision ID	ASIC ID	Siemens ID defined by TOS	Drive LOW	PERIPHID4(3:0) (Continuation code)	PERIPHID2(2:0) (ID-Code)	PERIPHID1(7:4) (ID-Code)	Drive HIGH
0x0	0x2	0x2F	0x0	0x0	0x1	0x8	0x1

3.6 PHY Wiring

3.6.1 PHY-TX Wiring

Observe the following design recommendations for the UTP (Unshielded Twisted Pair) interface:

- RX and TX pairs must be routed 100 Ω differential.
- Differential lengths for each pair must match in length.
- Transformer must be placed as close as possible to the ERTEC 200P-3 ASIC.
- Center tap of transformer must be connected with 10 Ω series resistor to 3.3V_Analog.
- 49.9 Ω termination resistors must be placed as close as possible to the ERTEC 200P-3 ASIC.
- Analog signals must be placed referenced to analog ground plane or common plane (same as digital) and must not be coupled with other signals.

Table 3-2: Electrical Characteristics Twisted Pair

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
100BASE-TX, 10BASE-T Transmitter						
Output common mode voltage	$V_{OCM,TP}$	with termination	0.65 * V_{DDIOA}		V_{DDIOA}	V
Differential Output Voltage Positive polarity	$V^{+}_{out\_10}$	10BASE-T 100Ohm term at transformer secondary side drive $V^{+}_{out\_10}$	2.2	2.5	2.8	Vp
Differential Output Current Positive polarity $I^{+}_{TP\_TX\_P\_10}$ - $I^{+}_{TP\_TX\_N\_10}$	I^{+}_{o10}	10BASE-T drive $V^{+}_{out\_10}$	-112	-100	-88	mA
Output current into TP_TX_P Positive polarity	$I^{+}_{TP\_TX\_P\_10}$	10BASE-T drive $V^{+}_{out\_10}$ $V_{TP\_TX\_P}$ > 1V	2.2	2.5	2.8	mA
Output current into TP_TX_N Positive polarity	$I^{+}_{TP\_TX\_N\_10}$	10BASE-T drive $V^{+}_{out\_10}$ $V_{TP\_TX\_N}$ > 1V	90	102.5	115	mA
Differential Output Voltage Negative polarity	$V^{-}_{out\_10}$	10BASE-T 100Ohm term at transformer secondary side drive $V^{-}_{out\_10}$	-2.8	-2.5	-2.2	Vp
Differential Output Current Negative polarity $I^{-}_{TP\_TX\_P\_10}$ - $I^{-}_{TP\_TX\_N\_10}$	I^{-}_{o10}	10BASE-T, drive $V^{-}_{out\_10}$	88	100	112	mA
Output current into TP_TX_P Negative polarity	$I^{-}_{TP\_TX\_P\_10}$	10BASE-T drive $V^{-}_{out\_10}$ $V_{TP\_TX\_P}$ > 1V	90	102.5	115	mA
Output current into	$I^{-}_{TP\_TX\_N\_10}$	10BASE-T	2.2	2.5	2.8	mA

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
TP_TX_N Negative polarity		drive $V^{-}_{out\_10}$ $V_{TP\_TX\_N} > 1V$				
Differential Output Current Mid value $I^{M}_{TP\_TX\_P\_10} - I^{M}_{TP\_TX\_N\_10}$	I^{M}_{o10}	10BASE-T, mid value	-5	0	5	mA
Output current into TP_TX_P	$I^{M}_{TP\_TX\_P\_10}$	10BASE-T mid value $V_{TP\_TX\_P} > 1V$	46.2	52.5	58.8	mA
Output current into TP_TX_N	$I^{M}_{TP\_TX\_N\_10}$	10BASE-T mid value $V_{TP\_TX\_P} > 1V$	46.2	52.5	58.8	mA
Differential Output Voltage Positive polarity	V^{+}_{out}	100BASE-TX 100Ohm term at transformer secondary side drive V^{+}_{out}	0.95		1.05	Vp
Differential Output Current Positive polarity $I^{+}_{TP\_TX\_P\_100} - I^{+}_{TP\_TX\_N\_100}$	I^{+}_{o100}	100BASE-TX drive V^{+}_{out}	-42.4		-40.74	mA
Output current into TP_TX_P	$I+_{TP\_TX\_P\_100}$	100BASE-TX drive V^{+}_{out} $V_{TP\_TX\_P} > 2V$	2.8	-	3.5	mA
Output current into TP_TX_N	$I+_{TP\_TX\_N\_100}$	100BASE-TX drive V^{+}_{out} $V_{TP\_TX\_P} > 2V$	43.9	-	45.9	mA
Differential Output Voltage Negative polarity	V^{-}_{out}	100BASE-TX 100Ohm term at transformer secondary side	-0.95	-	-1.05	Vp
Differential Output Current Negative polarity $I^{-}_{TP\_TX\_P\_100} - I^{-}_{TP\_TX\_N\_100}$	I^{-}_{o100}	100BASE-TX drive V^{-}_{out}	40.74	-	42.4	mA
Output current into TP_TX_P	$I^{-}_{TP\_TX\_P\_100}$	100BASE-TX drive V^{-}_{out} high value	43.9	-	45.9	mA

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
		$V_{TP\_TX\_P}$ >2V				
Output current into TP_TX_N	$I^{-}_{TP\_TX\_N\_100}$	100BASE-TX drive V^{-}_{out} low value $V_{TP\_TX\_N}$ >2V	2.8	-	3.5	mA
Differential Output Current Mid value $I^{M}_{TP\_TX\_P\_100} - I^{M}_{TP\_TX\_N\_100}$	I^{M}_{o100}	100BASE-TX mid value	-2	0	2	mA
Output current into TP_TX_P	$I^{M}_{TP\_TX\_P\_100}$	100BASE-TX mid value $V_{TP\_TX\_P}$ >2V	23.1	-	25.7	mA
Output current into TP_TX_N	$I^{M}_{TP\_TX\_N\_100}$	100BASE-TX mid value $V_{TP\_TX\_P}$ >2V	23.1	-	25.7	mA
Amplitude symmetry $\lvert I^{+}_{o100}/I^{-}_{o100} \rvert$	Amp_{Sym_100}	100BASE-TX 100Ohm term at transformer secondary side	0.98	-	1.02	-
Rise time (positive)	t_{or100}	100BASE-TX MLT-3 10%-90%	3	4	5	ns
Fall time (negative)	t_{of100}	100BASE-TX MLT-3 90%-10%	3	4	5	ns
Rise time symmetry (positive)	S_{r100}	100BASE-TX			500	ps
Fall time symmetry (negative)	S_{f100}	100BASE-TX			500	ps
Rise to fall time symmetry	S_{rf100}	100BASE-TX			500	ps
100BASE-TX, 10BASE-T Receiver						
Input common mode voltage	$V_{ICM,TP}$		0.9 * V_{DDIOA}		V_{DDIOA}	V

Figure 3-6 shows a typical UTP circuit with separate center taps on the magnetic.

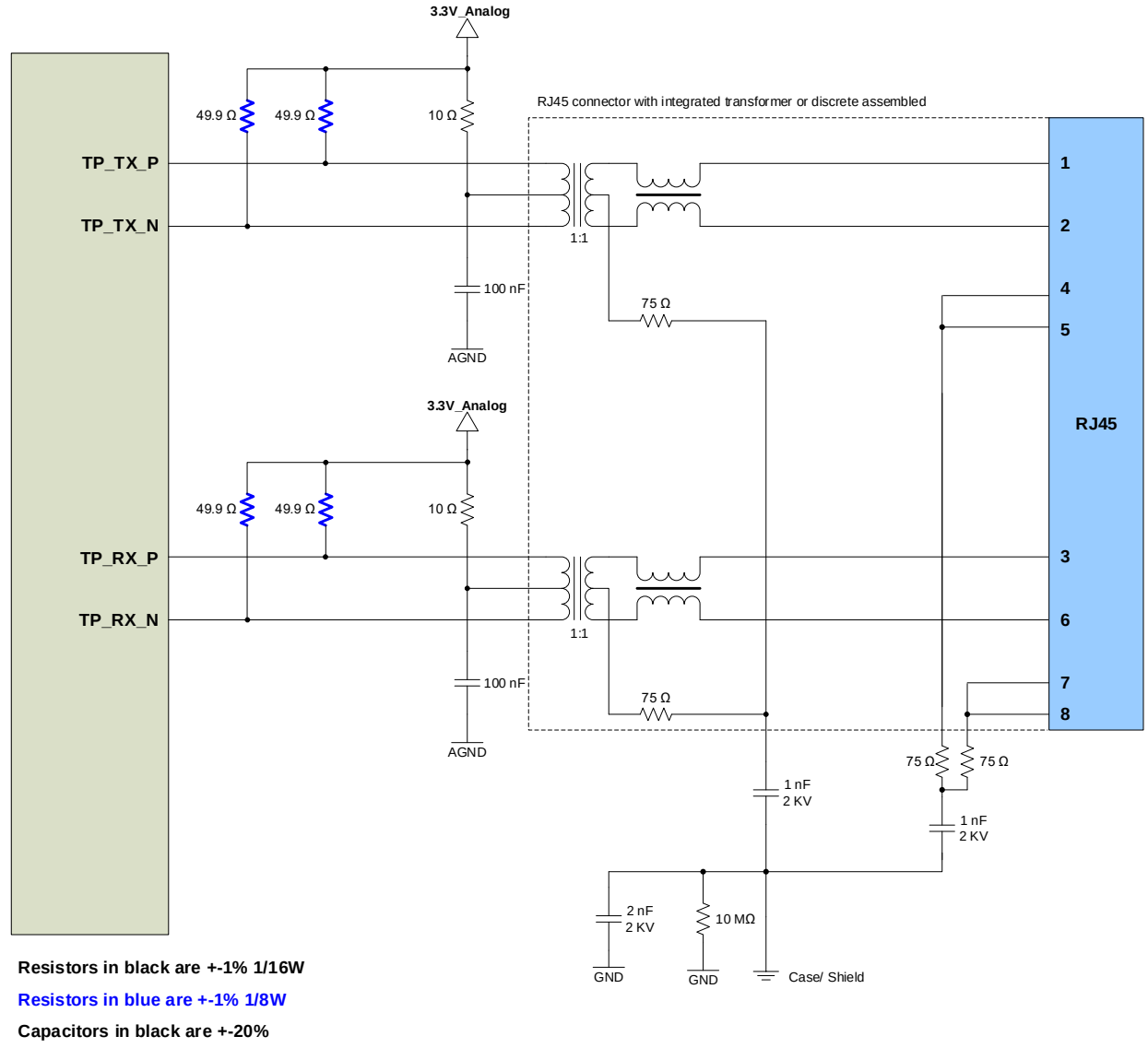

Figure 3-6: PHY-TX Wiring

Note

UTP interface must fulfill ANSI X3.263-1995 FDDI specification.

3.6.2 PHY-TX Wiring – UTP port not used

Unused UTP port should be left open.

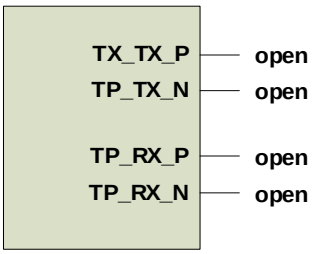

Figure 3-7: UTP circuit unused

3.6.3 PHY-FX Wiring

Observe the following design recommendations for the FX interface:

- It is strongly recommended to use PROFINET compliant POF Transceiver QFBR-5978AZ from company Avago.
- RX and TX pairs (LVPECL) must be routed 100 Ω differential.
- Differential lengths for each pair must match in length.
- Transceiver must be placed as close as possible to the ERTEC 200P-3 ASIC.
- The RX termination (130 Ω Pull-up and 82 Ω Pull-down) must be placed as close as possible to the ERTEC 200P-3 ASIC.
- RX and TX power supply on transceiver must be filtered separately.
- Pay attention to level translation between transceiver SD pin and ERTEC 200P-3 ASIC PHY input, see recommended circuit in Figure 3-8.
- Signals must be placed referenced to digital ground plane or common plane and must not be coupled with other signals.

Table 3-3: Electrical Characteristics Fiber

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Common Mode Voltage	$V_{ICM,FX}$	with termination	0.36 * V_{DDIOD}	82 / (82 + 130) * V_{DDIOD}	0.47 * V_{DDIOD}	V
Data input swing differential peak to peak	$V_{idiff,pp,FX}$		0.3	1.6	2.20	V
Data input low, single-ended	$V_{il,FX}$		0.5	0.876	1.5	V
Data input high, single- ended	$V_{ih,FX}$		1.1	1.676	2.15	V
Duty cycle distortion	$dcd_{i,FX}$		-1		1	ns
Data dependent input jitter	$ddj\_rms_{i,FX}$	PRBS7 input pattern	0		1.5	ns
Data differential input rise time	$t_{ir,FX}$	10% to 90%			2.2	ns
Data differential input fall time	$t_{if,FX}$	90% to 10%			2.2	ns
Common mode output voltage	$V_{OCM,FX}$	with termination	V_{DDIOD} – 1.2	V_{DDIOD} – 1	V_{DDIOD} – 0.8	V
Data output swing differential peak to peak	$V_{odiffpp,FX}$	with termination	0.95		1.6	V
Data output low	$V_{ol,FX}$	with termination	V_{DDIOD} – 1.54	V_{DDIOD} – 1.33	V_{DDIOD} – 1.13	V
Data output high	$V_{oh,FX}$	with termination	V_{DDIOD} – 0.77	V_{DDIOD} – 0.66	V_{DDIOD} – 0.56	V
Output current into FX_TX_P Positive polarity	$I+_{FX\_TX\_P}$	without termination drive $V_{oh,FX}$ $V_{FX\_TX\_P} > V_{OCM,FX,min}$	-10	0	10	uA
Output current into FX_TX_N Positive polarity	$I+_{FX\_TX\_N}$	without termination drive $V_{ol,FX}$ $V_{FX\_TX\_P} > V_{OCM,FX,min}$	15	19.5	25	mA
Output current into FX_TX_P	$I-_{FX\_TX\_P}$	without termination	15	19.5	25	mA

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Negative polarity		drive $V_{ol,FX}$ $V_{FX\_TX\_P} > V_{OCM,FX,min}$				
Output current into FX_TX_N Negative polarity	$I_{-FX\_TX\_N}$	without termination drive $V_{oh,FX}$ $V_{FX\_TX\_P} > V_{OCM,FX,min}$	-10	0	10	uA
Data output rise time	$t_{or,FX}$	10% to 90%, C_{Lmax} = 20 pF, $C_L = C_P + C_N$, $0.9*C_P < C_N < 1.1*C_P$	0		1.9	ns
Data output fall time	$t_{of,FX}$	90% to 10%, C_{Lmax} = 20 pF, $C_L = C_P + C_N$, $0.9*C_P < C_N < 1.1*C_P$	0		1.9	ns
Data output differential rise/fall time symmetry	$t_{orfsym,FX}$	$t_{orfsym,FX} = t_{or,FX} - t_{of,FX}$; $t_{or,FX} < 1$ ns & $t_{of,FX} < 1$ ns	-100		100	ps
Data output differential rise/fall time symmetry	$t_{orfsym,FX}$	$t_{orfsym,FX} = t_{or,FX} - t_{of,FX}$; $t_{or,FX} \geq 1$ ns & $t_{of,FX} \geq 1$ ns	-0.1 * $t_{or,FX}$		0.1 * $t_{or,FX}$	ns
Data dependent jitter	$ddj\_rms_{o,FX}$	PRBS7 output pattern	0		1.3	ns
Data differential overshoot	$V_{OS,FX}$		0		0.1 * $V_{odiffpp,FX}$	V
Common Mode Voltage Ripple	$V_{OCM,Ripple,pp,FX}$	Peak-to-peak value of $(V_{oh,FX} + V_{ol,FX}) / 2$	0		0.2	v

Figure 3-8 shows the recommended FX circuit.

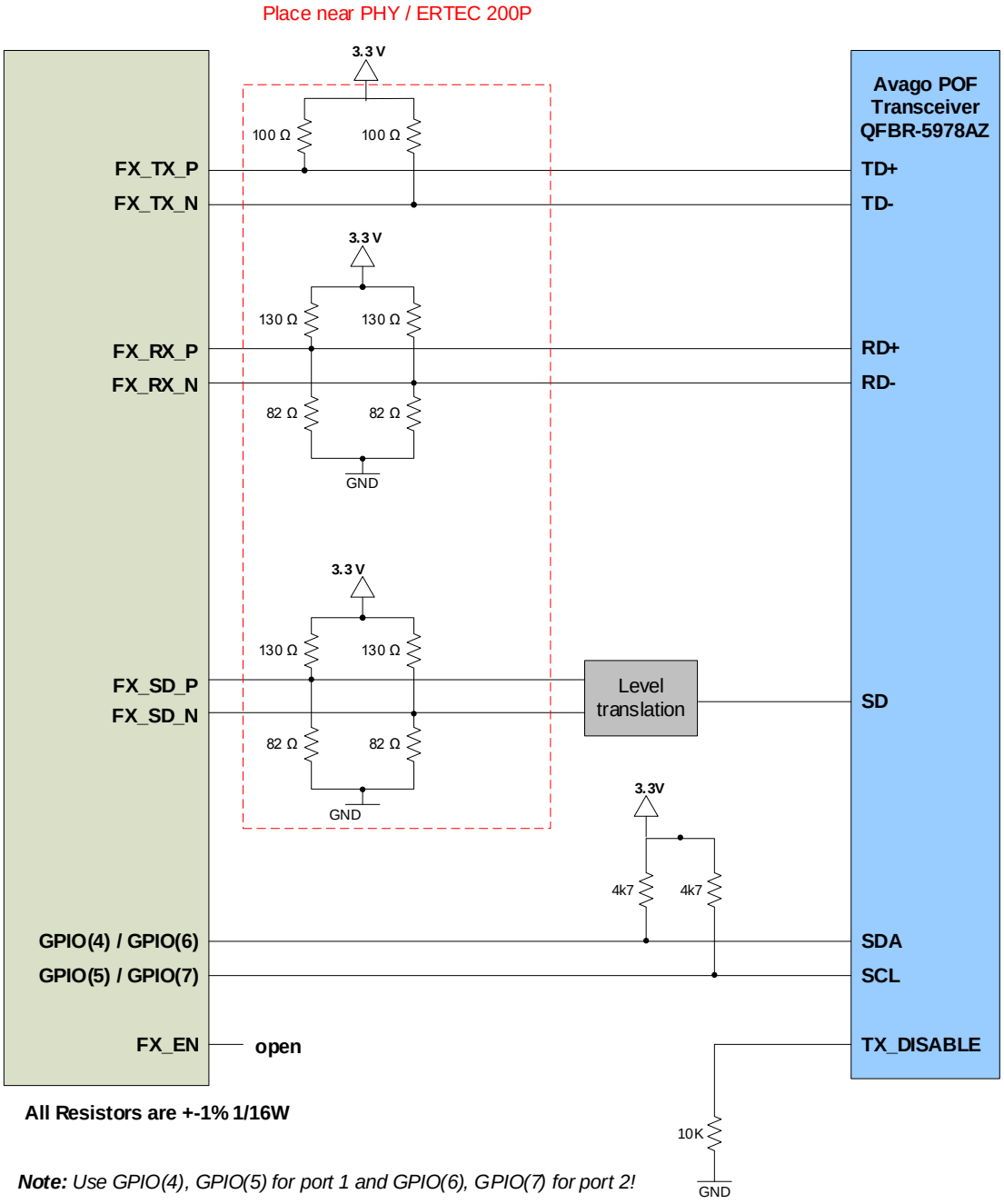

Figure 3-8: PHY FX ciruit

3.6.4 PHY-FX Wiring – FX circuit not used

FX_TX_P/N signals on unused FX port should be left open, **FX_RX_P/N** and **FX_SD_P/N** inputs must be connected directly to GND, the GPIOs can be configured for alternate function.

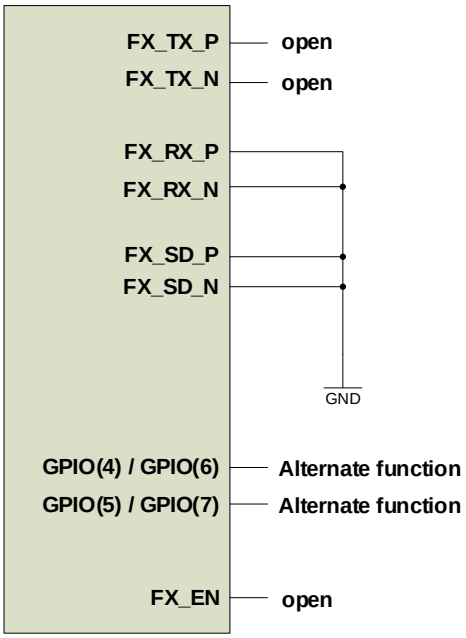

Figure 3-9: PHY FX circuit unused pins

3.6.5 PHY-SD Wiring – Avago QFBR-5978AZ

The Avago QFBR-5978AZ has a single ended output and ERTEC 200P-3 ASIC has a differential LVPECL input and optionally also a CMOS input via GPIO (see chapter 3.6.5.2).

3.6.5.1 PxSD circuit

The following level translation circuit is recommended **for direct connection of FX_SD_P/N signals**. Comparator shall be placed near transceiver and PECL driver near ERTEC 200P-3 ASIC. The 3.3 V supply voltage tolerance for **POF transceiver and SD level translation circuit** is limited to **+- 5%.**

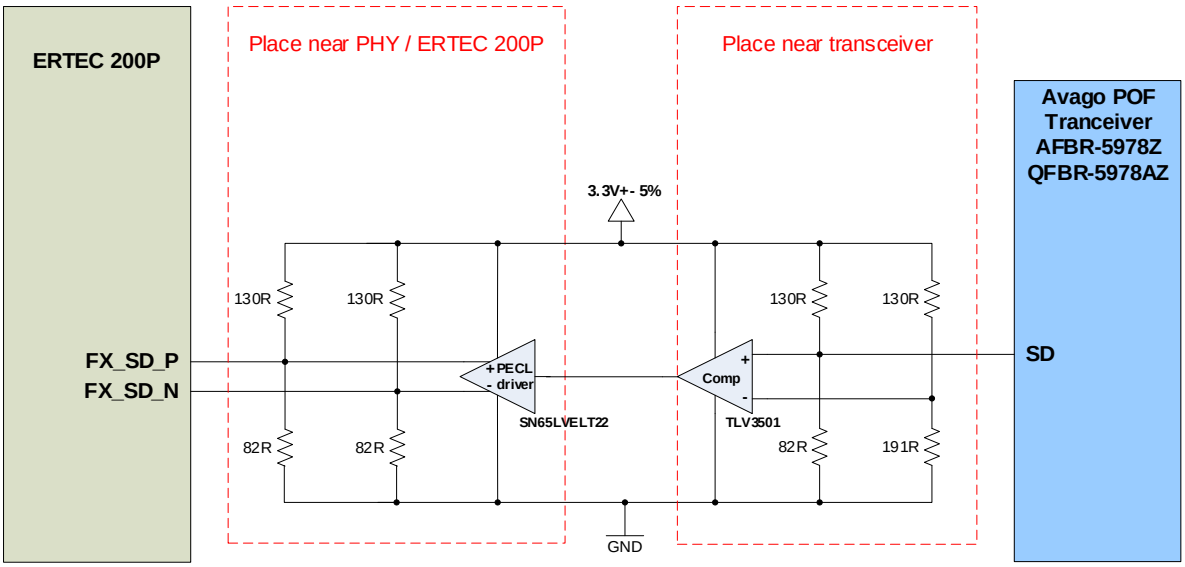

Figure 3-10: SD level translation circuit (FX_SD_P/N)

3.6.5.2 GPIO circuit

The following level translation circuit is recommended **when GPIOs are used**. Comparator must be placed near transceiver. The 3.3 V supply voltage tolerance for **POF transceiver** is limited to **+- 5%**.

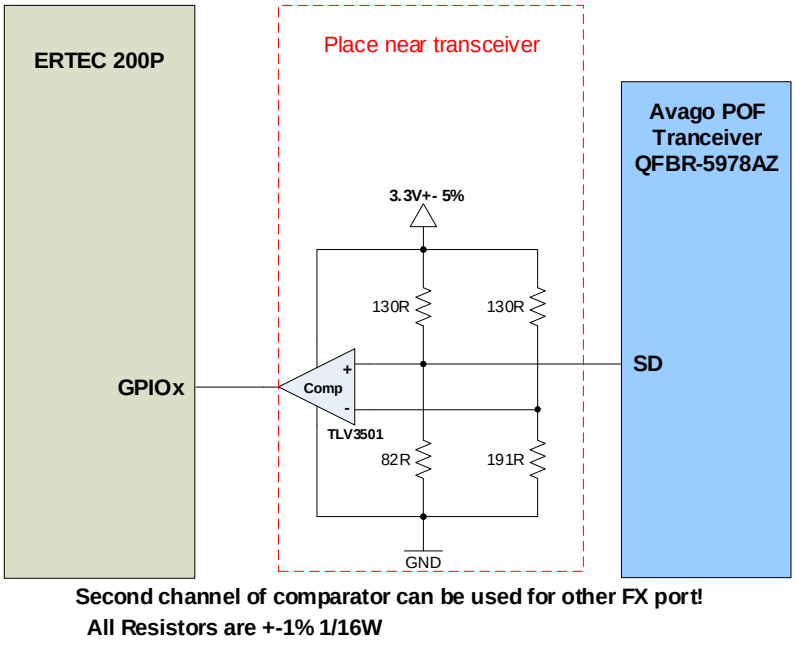

Figure 3-11: SD level translation circuit (GPIO)

3.7 Wiring of unused pins

The following applies in general:

- IN and INOUT pins that do **not** have an internal pull resistor must be connected to an external pull resistor.
- If the internal Pull-up/down resistor of the GPIOs is **deactivated**, it must be activated by the SW or an external Pull-up/down resistor must be connected.

Table 3-4: Recommendation for handling special function signals

Signal	Signal description	Dir	Function description	Ball
TEST	IC-Test-Mode	in	IC Test Mode Select signal for ASIC test. For normal operation this pin must be connected to GND.	F12
TMC1	Testmode_1	in	Test Mode Control Signal for ASIC test. For normal operation this pin must be connected to GND.	R9
TMC2	Testmode_2	in	Test Mode Control Signal for ASIC test. For normal operation this pin must be connected to GND.	F7
TACT	TESTACT-TAP-RESET	in	Special Test Mode TAP Controller Used for Boundary scan test. For normal operation this pin must be connected to GND.	F9
TAP_SEL	TAP Select	in	TAP Select Used for Boundary scan test. For normal operation this pin must be connected to GND.	E14
P1FXEN	Port 1 Fiber Optic Enable	out	Port 1 Fiber Optic Enable This pin is not used and must be unconnected. The Fiber Optic transceiver must be enabled all the time by proper pull resistor.	V12
P2FXEN	Port 2 Fiber Optic Enable	out	Port 2 Fiber Optic Enable This pin is not used and must be unconnected. The Fiber Optic transceiver must be enabled all the time by proper pull resistor.	A13
CLK_O_SDRAM 2	EMC SDRAM Clock Out	bi	Clock Output SDRAM 2 In normal operation this signal is connected to second SDRAM, upper 16 Bit. If only one SDRAM is implemented an external Pull-up resistor must be connected.	M15

3.8 Operating Conditions

3.8.1 Absolute Maximum Ratings

Table 3-5: Absolute maximum ratings

Parameter	Symbol	Condition/Remark	Min	Typ.	Max	Unit
I/O supply voltage to GND	VDD_IO		-0.3		3.93	V
Core supply voltage to GND	VDD_CORE		-0.3		1.6	V
PLL_A digital supply voltage	AVDD_PLLA		-0.3		1.6	V
PLL_A analog supply voltage, filtered	AVDDHV_PLLA		-0.3		3.93	V
PLL_B digital supply voltage	AVDD_PLLB		-0.3		1.6	V
PLL_B analog supply voltage, filtered	AVDDHV_PLLB		-0.3		3.93	V
I/O voltage to GND		I/Os connected to LNBD12MDSTPS33 buffers	-0.3		3.93	V
		I/Os connected to ZLLNBD12MDSTPS33 buffers	-0.3		3.93	
		I/Os connected to LNBINST33 input buffers	-0.3		3.93	
Oscillator input	XCLK1	connected to LNAINHV buffer	-0.3		3.93	V
Oscillator output	XCLK2	connected to LNOSCMD33O buffer	-0.3		3.93	V

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3.8.2 Conditions of Operation

Table 3-6: Operating conditions

Parameter	Symbol	Condition/Remark	Min	Typ.	Max	Unit
Pin capacitance	C_P	LNBD12MDSTPS33 with PAD		2.2		pF
		ZLLNBD12MDSTPS33 with PAD		2.2		
		ZLLNBD12MDSTPS33X2 with PAD		4.4		
		LNBINST33 with PAD		1.8		
		LNOSCMD33 with PAD		4.0		
Supply voltages						
Core voltage supply	VDD_CORE		1.045	1.1	1.155	V
I/O voltage supply	VDD_IO		1.62	1.8	1.89	V
			2.97	3.3	3.465	
PLL_A digital/analog supply voltage	AVDD_PLLA		1.045	1.1	1.155	V
	AVDDHV_PLLB		1.62	3.3	3.63	
PLL_B digital/analog supply voltage	AVDD_PLLA		1.045	1.1	1.155	V
	AVDDHV_PLLB		1.62	3.3	3.63	
Core voltage rise time	t_{r,VDD_CORE}		10		100000	µs
I/O voltage rise time	$tr_{,VDD\_IO}$		10		100000	µs
Supply currents						
Core supply current	I_{VDD_CORE}	typ=TT/1.1V/25°C max=FF/1.155V/112°C		67.89	227.59	mA
I/O supply current	I_{VDD_IO}	EMC/XHIF=1.8V typ=TT/1.8V/112°C max=FF/3.465V/1.89V/112°C		50.76	53.30	mA
PLL supply current	I_{AVDD_PLLA}	FVCO=500MHz		0.8	1.56	uA/ MHz
	$I_{AVDDHV\_PLL\_A}$			0.30	0.35	mA

Parameter	Symbol	Condition/Remark	Min	Typ.	Max	Unit
	$I_{AVDD\_PLLA\_B}$	VFCO=1600MHz		0.8	1.56	uA/ MHz
	$I_{AVDDHV\_PLL\_B}$			1.72	2.02	mA
Oscillator						
XTAL1 low level input voltage	V_{IL}		-0.3		0.3*VDDIO	V
XTAL1 high level input voltage	V_{IH}		0.7*VDDIO		VDDIO+0.3	V
XTAL1 rise/fall time	t_{RF}				16	ns
external clock source frequency	f_{IN}			25		MHz
GPIOs						
Input low level	V_{IL}	LNBD12MDSTPS33 LNBINST33	-0.3		0.3*VDDIO	V
Input high level	V_{IH}	LNBD12MDSTPS33 LNBINST33	0.7*VDDIO		VDDIO+0.3	V
Schmitt Trigger high to low threshold	V_N	LNBD12MDSTPS33 LNBINST33	0.25*VDDIO		0.65*VDDIO	V
Schmitt Trigger low to high voltage	V_P	LNBD12MDSTPS33 LNBINST33	0.35*VDDIO		0.75*VDDIO	V
Schmitt Trigger Hysteresis	V_H	LNBD12MDSTPS33 LNBINST33	0.1*VDDIO		0.5*VDDIO	V
Output low level	V_{OL}	LNBD12MDSTPS33 IOL=2mA(VDDIO min3.0 max3.6 DSTR0=0,DSTR1=0)	-		0.4	V
		LNBD12MDSTPS33 IOL=4mA(VDDIO min3.0 max3.6 DSTR0=1,DSTR1=0)	-		0.4	

Parameter	Symbol	Condition/Remark	Min	Typ.	Max	Unit
		LNBD12MDSTPS33 IOL=100uA IOL=8mA(VDDIO min3.0 max3.6 DSTR0=0,DSTR1=1)	- -		0.15*VDDIO[1] 0.4	
		LNBD12MDSTPS33 IOL=12mA(VDDIO min3.0 max3.6 DSTR0=1,DSTR1=1)	-		0.4	
Output high level	V_{OH}	LNBD12MDSTPS33 IOH=-2mA(VDDIO min3.0 max3.6 DSTR0=0,DSTR1=0)	2.4		-	V
		LNBD12MDSTPS33 IOH=-4mA(VDDIO min3.0 max3.6 DSTR0=1,DSTR1=0)	2.4		-	
		LNBD12MDSTPS33 IOH=-100uA IOH=-8mA(VDDIO min3.0 max3.6 DSTR0=0,DSTR1=1)	0.85*VDDIO[2] 2.4		- -	
		LNBD12MDSTPS33 IOH=-12mA(VDDIO min3.0 max3.6 DSTR1=1,DSTR1=1)	2.4		-	
Pull-up	R_{PU}	LNBD12MDSTPS33 LNBINST33	20		80	kΩ
Pull-down	R_{PD}	LNBD12MDSTPS33 LNBINST33	20		80	kΩ
Input current	I_{IN}	LNBD12MDSTPS33 LNBINST33 Input voltage = 0 Pull-up off	-10		10	µA
		LNBD12MDSTPS33 LNBINST33 Input voltage = 3.449 Pull-down off	-10		10	

[1] V_{OL}: The GPIO buffer meets both JESD8-23 (LVCMOS) and JESD8C (LVTTL) standards. JESD8-23 specifies a maximum V_{OL} level for 100µA load (0.15*VDDIO) and JESD8C for 8mA load (0.4V).

[2] V_{OH}: The GPIO buffer meets both JESD8-23 (LVCMOS) and JESD8C (LVTTL) standards. JESD8-23 specifies a minimum V_{OH} level for -100µA load (0.85*VDDIO) and JESD8C for -8mA load (2.4V).

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Parameter	Symbol	Condition/Remark	Min	Typ.	Max	Unit
		LNBD12MDSTPS33 LNBINST33 Input voltage = 0 Pull-up 50kΩ	-200		10	
		LNBD12MDSTPS33 LNBINST33 Input voltage = 3.449 Pull-down = 50kΩ	-10		200	
Input rise time	t_r	LNBD12MDSTPS33 LNBINST33 normal CMOs input			16	ns
		Schmitt Trigger input			16	ns
Input fall time	t_f	LNBD12MDSTPS33 LNBINST33 normal CMOs input			16	ns
		Schmitt Trigger input			16	ns

3.8.3 Ambient Conditions

Table 3-7: Ambient conditions

Parameter	Symbol	Condition/Remark	Min	Typ.	Max	Unit
Ambient operating temperature	T_A		-40		85	°C
Case operating termperature	T_C		-40		105	°C
Top of package temperature at center	T_T		-40		105	°C
Junction operating temperature	Tj		-40		112	°C

3.8.4 Power Up

There is no set order for switches on the supply voltages. However, all must be activated within a period of 200 ms.

3.8.5 Wiring of CTRL-STBY

To ensure that the outputs remain at high-impedance upon power up, CTRL_STBY function is connected to the XRESET pin.

3.8.6 Power-Up Sequence (PLL)

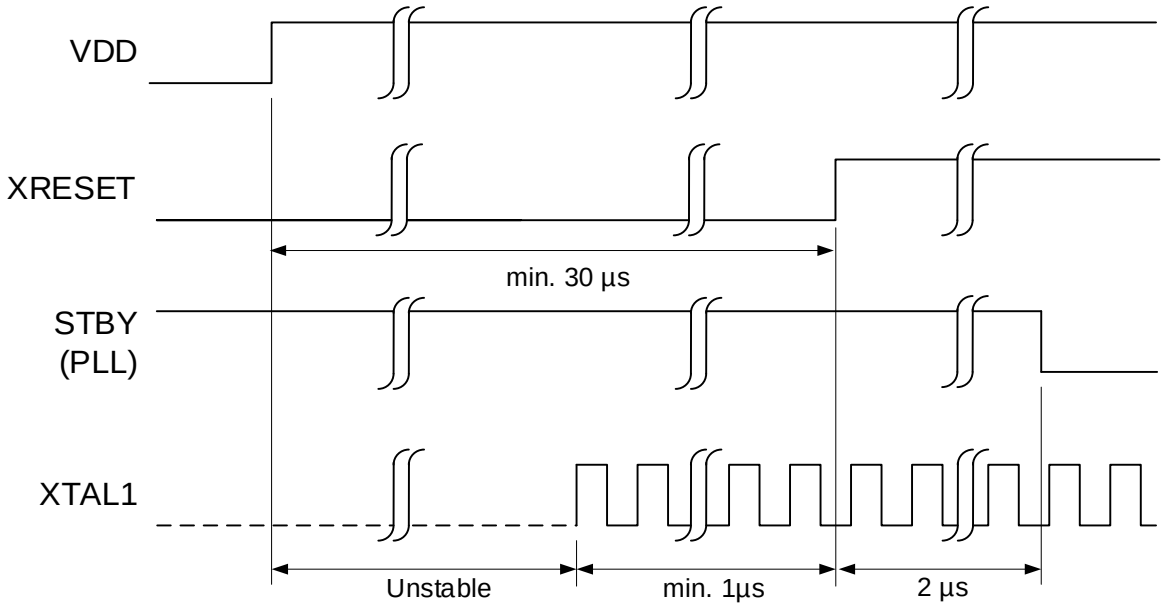

Figure 3-12: Power-Up Sequence (PLL)

The standby signal (STBY) to the PLL is an extension of XRESET by 30 µs.

3.8.7 PLL Behavior

3.8.7.1 Following quartz break

If the ext. quartz breaks, i.e. XTAL1/2 are

- open
- clamped to '0'
- clamped to '1',

a frequency of 100 MHz … 300 MHz is established at the PLL output (free-running frequency).

3.8.7.2 External filtering

For optimal jitter performance, it is suggested to place external decoupling capacitors between each PLL power supply and VSS. This is most important for AVDDHV_PLL, which is sensitive to low frequency noise and can only be effectively filtered off-chip. It is highly recommended to decouple AVDD_PLL as well. For optimal decoupling it is suggested to use at least one large capacitor (e.g. 4.7 µF) for each separate supply. Additionally, smaller capacitors (e.g. 100 nF or 10 nF) may be placed in parallel since the lead inductance of the large capacitor may be significant. The capacitors shall be placed with the smallest one closest to the chip, while larger capacitors can be placed further away. Capacitors with minimal lead inductance shall be selected. Ceramic-type capacitors work well. The capacitors shall be placed as close to the package pins as possible. No series impedance shall be added anywhere on the board, and impedance to the power supplies shall be minimized. Adding a series ferrite bead may help to attenuate high frequency noise. Commonly available ferrite beads may have only a few Ω at DC but have an impedance of several kΩ as low as 100 kHz.

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3.8.7.3 Upon temporary clock failure

With 30 ps (see chapter 3.3.3) the period jitter is within the specified range provided the recommended filter connections for AVDD decoupling are used.

If the reference clock for the ERTEC 200P-3 PLL fails, the frequency will change continuously until it reaches the final value after ca. 30 µs.

3.9 Power Dissipation

Worst case power dissipation, related to technology, temperature, and power supply.

(T_J = 112°C, Power supply + 5%)

Table 3-8: Power Dissipation with 1.8 V / 3.3 V, switchable IO set to 1.8 V

Use Case	Unit	**ERTEC 200P-3**
switchable I/O voltage	V	**1.8**
Core (CPUs, RAMs, Clock, Logic)	mW	262.9
Macros (PLLs)	mW	2.3
PN-PHY	mW	360
3.3 V I/Os	mW	23.9
1.8 V I/Os	mW	69.2
1.8 V / 3.3 V I/Os	mW	18.5
total		**736.8**

Table 3-9: Power Dissipation with 1.8 V / 3.3 V, switchable IO set to 3.3 V

Use Case	Unit	**ERTEC 200P-3**
switchable I/O voltage	V	**3.3**
Core (CPUs, RAMs, Clock, Logic)	mW	262.9
Macros (PLLs)	mW	2.3
PN-PHY	mW	360
3.3 V I/Os	mW	23.9
1.8 V I/Os	mW	69.2
1.8 V / 3.3 V I/Os	mW	62.1
total		**780.4**

3.10 Interface Changes from ERTEC 200P-2 to ERTEC 200P-3

Table 3-10: Interface Changes

Interface Changes	ERTEC 200P-3	ERTEC 200P-2
CLK/RES		
CLKP_A renamed to XTAL1	XTAL1	CLKP_A
CLKP_B renamed to XTAL2	XTAL2	CLKP_B
TEST		
CTRL_STBY0/1/2 signals are removed in ERTEC 200P-3	-	CTRL_STBY0
	-	CTRL_STBY1
	-	CTRL_STBY2
L/A_PHY1/2		
No changes to interface		
PN_PHY		
No changes to interface		
EMC		
CLK_O_BF0/1/2 signals are removed in ERTEC 200P-3	-	CLK_O_BF0
	-	CLK_O_BF1
	-	CLK_O_BF2
CLK_I_BF signal is removed in ERTEC 200P-3	-	CLK_I_BF
JTAG		
No changes to interface		
GPIO		
No changes to interface		
XHIF		
No changes to interface		
Power/GND		
Power and Ground has changed massively from ERTEC 200P-2 to ERTEC 200P-3 and has to be redesigned.		

4 Design Considerations

4.1 Design Recommendations

Note

Regardig recommendations for board design, e.g., power supply please refer to manual “Evaluation Board ERTEC 200P-3”.

4.1.1 Design Recommendations for ERTEC 200P-3 EMC Bus

Note

The following design recommendations apply to the use of EMC with 1.8 V.

4.1.1.1 Recommended EMC Settings

Table 4-1: Recommended EMC settings

	Register	Legacy mode - default	Legacy mode - fast
EMC	ASYNC_WAIT_CYCLE_CONFIG	0x40000080 (d)	
EMC	SDRAM_CONFIG	0x00002521	
EMC	SDRAM_REFRESH	0x000003CF	
EMC	ASYNC_BANK0	0x3FFFFFF2 (d)	0x0C302502
EMC	ASYNC_BANK1	0x3FFFFFF2 (d)	
EMC	ASYNC_BANK2	0x3FFFFFF2 (d)	
EMC	ASYNC_BANK3	0x3FFFFFF2 (d)	
EMC	EXTENDED_CONFIG	0x05B74600	
EMC	LPEMR	0x00000000 (d)	
EMC	BF_CONFIG	0x00000000 (d)	0x00000000 (d)
EMC	PM_CONFIG	0x0000003F (d)	0x0000003F (d)
EMC	RECOV_CONFIG	0x00000000 (d)	

Before initialization start, clocks for all chips must be enabled.

Note

Make sure that SDRAM_CONFIG register is written last when initializing EMC-SDRAM registers, because SDRAM Load Mode Register sequence is started when writing SDRAM_CONFIG.

4.1.1.2 Used SDRAM

The board simulation was done with the following SDRAM: Micron MT48H16M32LFB5-6 IT:C

Optionally, the following device can be used: ISSI ISS-IS42VM16320E-75B

Note

The E version of the ISSI is mandatory, earlier versions show incorrect behaviour.

4.1.1.3 Possible ERTEC 200P-3 EMC configurations

The EMC configuration is application-dependent, Figure 4-1 shows all possible configurations.

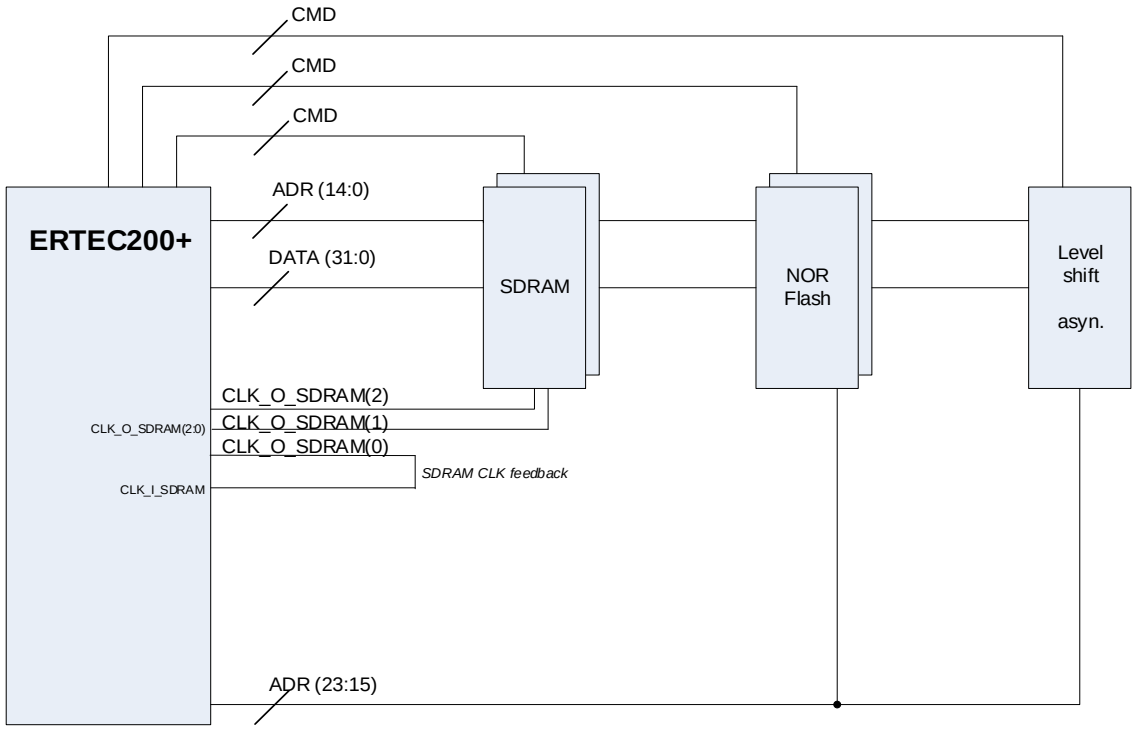

Figure 4-1: EMC Bus configurations

Mandatory clock signal assignment:

CLK_O_SDRAM(0) must be used as feedback clock source and therefore returned to CLK_I_SDRAM.

CLK_O_SDRAM[2:1] must be used for SDRAM clock source accordingly, so that every SDRAM device has a distinct source.

Note

CLK_O_SDRAM(0) must feedback to CLK_I_SDRAM even if only asynchronous devices are used, because read data is always latched in on ERTEC 200P-3 with CLK_I_SDRAM clock. Allowed velocity and impedance on all EMC transmission lines are:

	Velocity (µm / ps)	Impedance (ohm)
typical	150	60
bestcase	182	69
worstcase	137	51

4.1.1.4 ERTEC 200P-3 EMC recommendations

The recommended values below fulfill the bus configurations/ requirements for ERTEC 200P:

- Min/Max length configuration from driver to receiver

Table 4-2: Min/ max trace length

	Max length [mm]	Min length [mm]	Max # Vias
Address [0-14]	87	6	5
Address [15-23]/ CMD	84	6	4
Data	114	17	4
Clock/ CMD-DQMs	80	17	2

- All transmission lines must be routed on inner layers and referenced to GND.
- All Clocks to SDRAM and the associated feedback clock to ERTEC 200P-3 must match in length within 1 mm.
- All Clocks to Flash and the associated feedback clock to ERTEC 200P-3 must match in length within 1 mm.
- Clocks must always be routed as short as possible.
- Length matching between Data and Address to their corresponding clocks is not necessary.
- Clock must be shorter than the shortest Data line.
- If Address is less than 17 mm, clock max length is 17 mm (corner case).

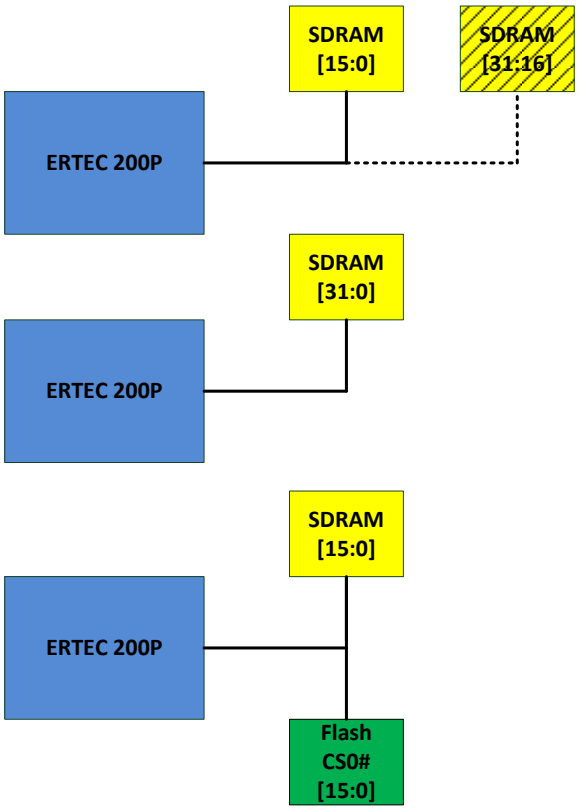

Figure 4-2: Use Case External Host

In the case of only one participant on ADR (address), Data or CMD line (see Table 4-2), an additional 8.2 pF capacitor is necessary on SDRAM signal lines (keep in mind the dedicated SDRAM signals).

4.1.1.5 SDRAM Write Timing

Figure 4-3 shows the SDRAM Write timing. Data/ address and command are output by ERTEC 200P-3 with the falling edge of CLK_O_SDRAM[1:2] clock and latched in with rising edge on SDRAM.

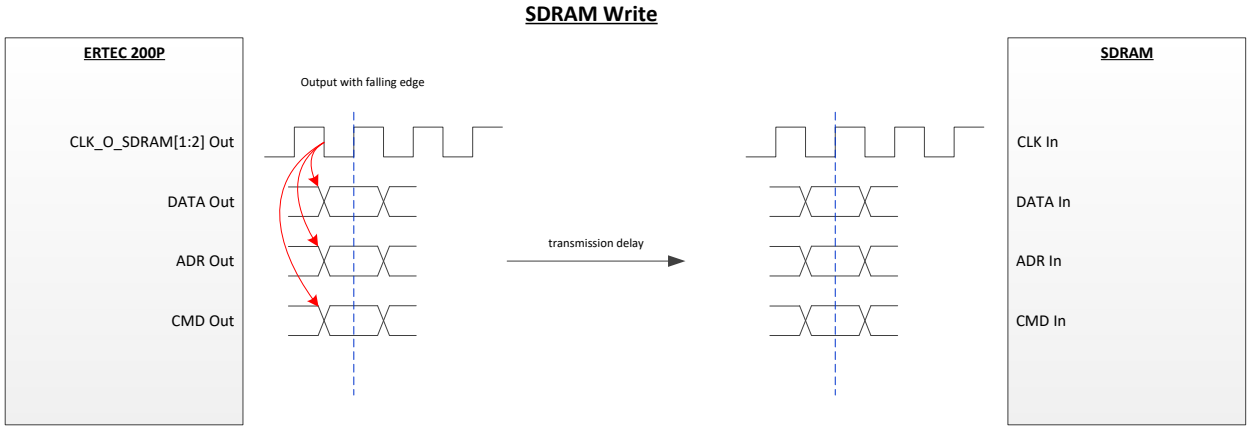

Figure 4-3: SDRAM Write Timing

4.1.1.6 SDRAM Read Timing

Figure 4-4 shows the SDRAM Read timing. Read data is latched in on ERTEC 200P-3 with rising edge of CLK_I_SDRAM.

Note

CLK_O_SDRAM(0) is not synchronous to CLK_O_SDRAM[1:2].

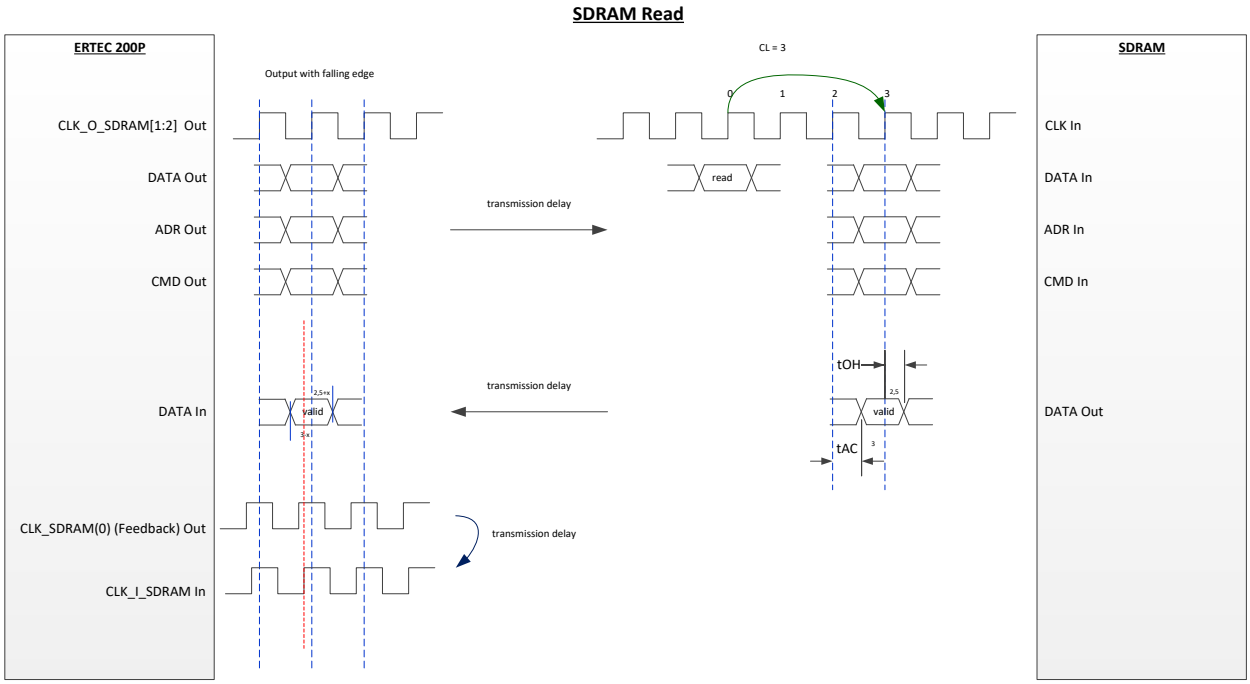

Figure 4-4: SDRAM Read Timing

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4.2 Clocking

4.2.1 Clock Generation and Distribution

The ERTEC 200P-3 clocks are provided by an internal PLL. Apart from the JTAG clock and the PHY clock, all clocks are generated by the integrated PLL.

Note

In ERTEC 200P-2 and earlier it was possible to provide a clock on pin BYP_CLK. This direct clock input has been removed from ERTEC 200P-3. However, pin BYP_CLK is still used for input of F_TAKT that is connected to the F-Timer.

Table 4-3: Overview of ERTEC 200P-3 clocks

Module	Clock Source	Frequency
ARM926EJ-S	PLL	250 MHz
AHB/EMC/ICU/HOST-IF/GDMA		125 MHz
PN-IP (except MAC MII/GMII)		125/250 MHz
PER_IF		125 MHz
APB		125 MHz
Octal SPI shell		125/250/500 MHz
EMC		125 MHz
PerIF		125 MHz
PN PHY		250 MHz
JTAG	JTAG clock	16/32 MHz
MAC MII/GMII / PHY	XTAL1 / external	25/125 MHz

4.2.2 Oscillator

See chapter 3.3.

4.2.3 External Clock Source

It is possible to use an external clock source instead of a quartz crystal as clock input for port XTAL1. In this case the port XTAL2 has to be left unconnected (open). For the requirements of XTAL1 see chapter 3.8.2.

4.2.4 PLL Power Supply

See chapter 3.8.7.2.

4.3 Reset

4.3.1 Power-On Reset Behaviour

For the Power-Up Sequence see chapter 3.8.6.

Access to internal resources of the ERTEC 200P-3 immediately after release of XRESET, e.g. over the XHIF interface, is only allowed after the internal initialization is finished (see also startup times in chapter 4.8.1).

Duration of initialization after deactivating the XRESET:

PLL-Standby-Time:	2 µs
PLL-Lockup-Time:	250 µs
EMC Init_Done[1]:	233 µs
Complete-Time:	**485 µs**

4.3.2 Strapping Pins

See chapter 2.2.1

4.3.3 Reset Structure

Table 4-4: ERTEC 200P-3 Reset Matrix

Destinations / Events	Degubber/Direction (Pin XSRST)	ARM926-Core (XRES_ARM926CORE)	ARM926-TCM Toplevel SCRB-TCM926 RES_SOFT_RETURN_ADDR (XRES_SYS)	PN-IP SCRB_PHY_CONFIG/STATUS SCRB_ASYN_RES_CTRL_REG Slice3 EN_WD_RES_PN (XRES_PN-IP)	Clock System (XRES_CTSRS)	JTAG_NTRST (EAS926)	SCRB_ASYN_RES_CTRL_REG Slice5	SCRB_RES_STAT_REG	OSIP (xres_ospi_shell_sctsrs)
PowerOn Reset ERTEC 200P-3 (Pin XRSET)	x/out	**x**	**x**	**x**	**x**	**x**	**x** (1h by PowerOn Reset)	**x** (4h by PowerOn Reset)	**x**
Debugger (Pin XSRST)	-/in	**x**	**x**	**x**	-	**x**	(set to 1)	(set to 4h)	**x**
JTAG Reset (Pin XTRST)	-/in	-	-	-	-	-	-	-	-
Watchdog Reset ARM926 + PN-IP (XRES_ARM926_WD + Logic)	-/in	**x** (Pulse duration)	**x** (Pulse duration)	**x** (Pulse duration)	-	-	(set to 1)	(set to 1h)	**x** (Pulse duration)
Watchdog Reset ARM926 without PN-IP (XRES_ARM926_WD + Logic)	-/in	**x** (Pulse duration)	**x** (Pulse duration)	-	-	-	-	(set to 1h)	**x** (Pulse duration)
SW Reset ERTEC 200P-3 without PN-IP/PHY (RES_SOFT)	-/in	**x** (Pulse duration)	**x** (Pulse duration)	-	-	-	-	(set to 2h)	**x** (Pulse duration)
SW Reset PN-IP/PHY (RES_SOFT_PN)	-/in	-	-	**x** (Pulse duration)	-	-	(set to 1)	-	-
Core Reset ARM926 RES_SOFT_ARM926_CORE	-/in	**x** (Pulse duration)	-	-	-	-		(set to 8h)	

Key:

destination/module is not affected by reset event

4.3.3.1 Asynchronous PowerOn Reset (XRESET)

The asynchronous[2] PowerOn reset is connected to the ERTEC 200P-3 with the XRESET pin. In response to this reset, the complete circuit (incl. clock system) of the ERTEC 200P-3 is reset and the configuration pins are latched. The XRESET reset must be applied steadily for at least 2 µs after a steady voltage is reached upon ERTEC 200P-3 startup (see 3.8.6). The PLL then starts up and after a further 250 µs, the PLL is locked. This time until the PLL locks is t_{LOCK}. Internally, the PowerOn reset phase is extended by this time (fixed setting; the PLL lock is not evaluated) and the clock system is not connected until the end of the startup phase. The internal reset remains active for a further 16 clocks after clock system startup to execute the reset internally. Debugger communication over the JTAG interface is not possible during this time.

[1] Parallel to the EMC Init_Done several internal SRAMs are also initialized during this time. The time for the EMC Init_Done is the longest. Therefore it is listed here.

[2] An asynchronous reset affects the reset input of a flip-flop. This reset is applied asynchronously but cleared synchronously.

Hardware monitors the locked state of the PLL. Two interrupts signal whether the PLL has lost its input clock (quartz break) or the PLL is not locked (PLL monitor, monitors input and output frequency). The two error states can also be queried directly from the SCRB register 'PLL_STAT_REG'.

A filter ensures that spikes <= 60 ns (best case) at the XRESET input are suppressed.

While the XRESET pin is active, the bidirectional pin XSRST is switched to output and activated. The debugger can then detect the PowerOn reset phase.

The PWRON_HW_RES bit in RES_STAT_REG is set during a PowerOn reset to allow an analysis of the reset event after a system restart. This bit is not affected by the reset function triggered. Upon restart, the software can read RES_STAT_REG.

4.3.3.2 Reset and Start-up Timing

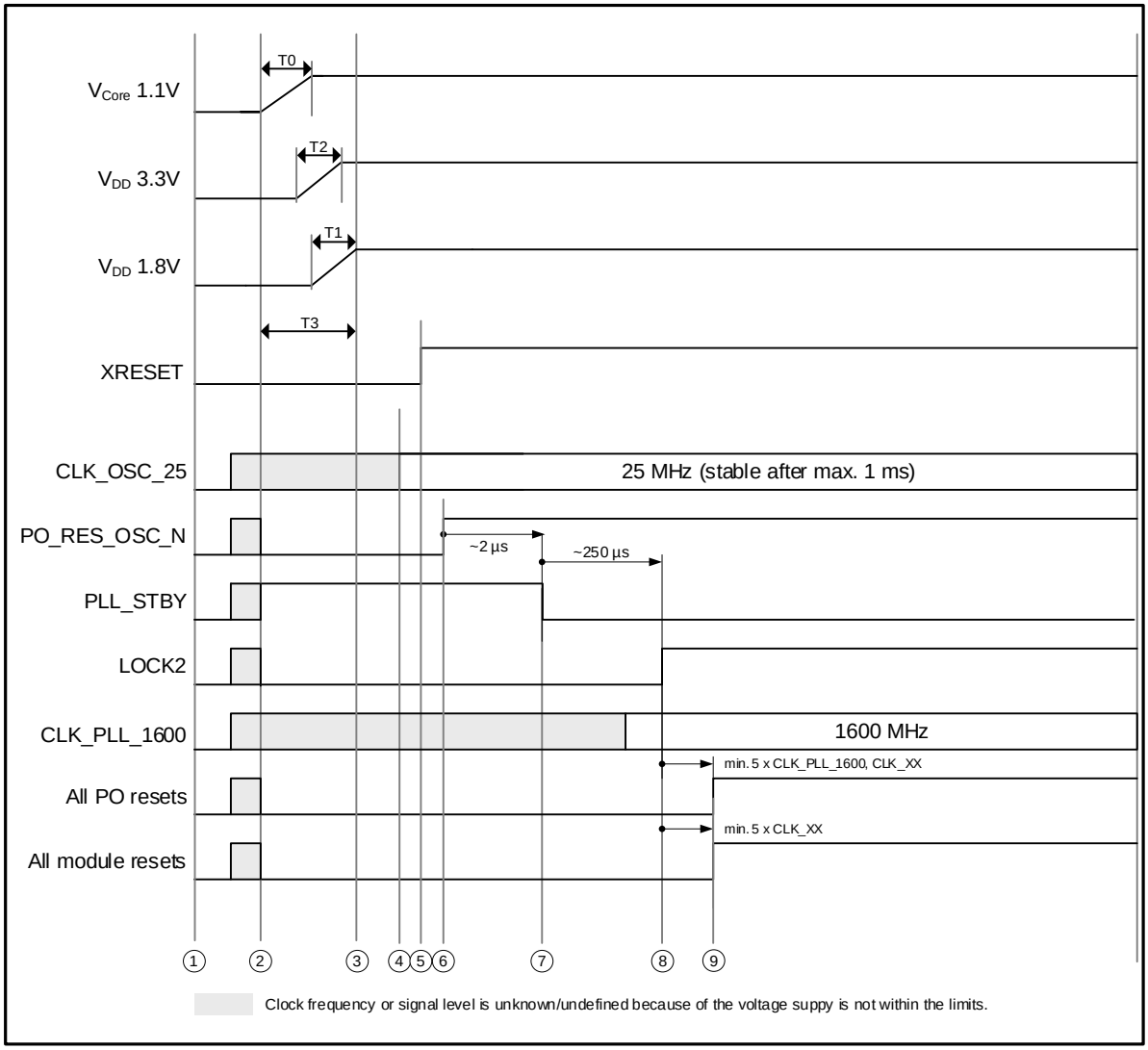

Figure 4-5: Reset and Start-up Timing

Key:

1. 0
2. The supply voltages start to ramp up. There is **no sequencing / no order** of the supplies required.

a. The core supply voltage is applied. The **ramp-up time** from 10% to 90% of the 1.1V voltage shall be between 10 µs and **100 ms (T0)**. (Same time requirement for ramp-down.)

b. The 1.8 V I/O supply voltage is applied. The **ramp-up** time from 10% to 90% of the 1.8V voltage shall be between 10 µs and **100 ms (T1)**. (Same time requirement for ramp-down.)

c. The 3.3 V I/O supply voltage is applied. The **ramp-up** time from 10% to 90% of the 3.3 V voltage shall be between 10 µs and **100 ms (T2)**. (Same time requirement for ramp-down.)

3. All power supplies are applied now.
   All power supplies shall be turned on (off) **within 200 ms (T3)**.
4. Oscillator output ist stable. Settling time is 1 ms (IO + external crystal + external components as recommended).
5. XRESET becomes inactive after all ASIC supply voltage and the oscillator outputs are stable.
6. PO_RES_OSC_N becomes inactive synchronous to the oscillator clock.
7. The PLLs require that the PLL_STBY signal (PLL-Input PD) is hold to logical 1 for at least 1 µs after the input frequency is stable. The timing is achieved with the Lock-Timer1 (2 µs).
8. The Lock-Timer2 gives the PLL enough time to setup the correct output frequency and allow for the required Fuse load time requested by the vendor. The Lock-Timer2 expires after approx. 250 µs.
9. All PO resets (beside the PO resets, which are used for the clock generation or at the clock monitor) and the module resets are inactive after five cycles of the appropriate clock.

4.3.3.3 Asynchronous Hardware Reset

The hardware reset is triggered with the XSRST pin by the external debugger. XSRST is a bidirectional IO cell with an open drain output. The complete internal logic is reset in the active XSRST phase, but not the clock system. The configuration pins are also **not** latched. During this hardware reset phase, the debugger can communicate with the embedded ICE logic over the JTAG interface, for example to load a breakpoint. Single stepping is therefore possible from the reset address.

The PWRON_HW_RES bit in RES_STAT_REG is set during a hardware reset to allow an analysis of the reset event after a system restart. This bit is not affected by the reset function triggered. Upon restart, the software can read RES_STAT_REG.

When booting after a hardware reset, the system uses the boot mode latched internally during the PowerOn reset.

XSRST is activated for the debugger if a PowerOn reset is active. XSRST must never be activated with 'RES_SOFT_ARM926_CORE', as this will prevent the debugger from running while one of the two cores is in reset state.

4.3.3.4 Asynchronous JTAG Reset

The JTAG reset is triggered with the XTRST pin by the external debugger. Only the Embedded ICE logic of the ARM926EJ-S is reset. To ensure that this Embedded ICE logic enters a defined state in operation without a debugger, it is also reset by a PowerOn reset (XRESET). An internal logic operation is implemented for this purpose.

4.3.3.5 Asynchronous ARM926 Watchdog Reset

The ARM926 watchdog reset is hardware monitoring of the software on the ARM926EJ-S. The basis for monitoring is a time set in the watchdog timer. This time starts to run when the watchdog is activated. If the timer is not retriggered to its initial value during this time, a watchdog reset (XRES_ARM926_WD) is triggered (output ARM926 watchdog: WD_XWDOUT1). If the watchdog function is enabled (WD_RES_FREI_ARM926) (see ASYN_RES_CTRL_REG), ERTEC 200P-3 is reset. The actual reset signal is related to a configurable pulse generation. The ARM926_WDOG_RES bit in RES_STAT_REG is

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set during an ARM926 watchdog reset to allow an analysis of the reset event after a system restart. This bit is not affected by the reset function triggered. Upon restart, the software can read RES_STAT_REG.

If, in a given application, you do not want expiry of the watchdog time to affect the operation of the PN-IP, you can exclude the PN-IP from the watchdog reset (EN_WD_RES_PN = 0 in ASYN_RES_CTRL_REG).

Note

The EN_WD_RES_PN bit is always set (PN-IP subject to ARM926 watchdog reset) if the PN-IP is reset (see Table 4-4). If an asynchronous software reset is to be generated by the SW for the PN-IP (see chapter 4.3.3.7), the SW must then set EN_WD_RES_PN = 0 again to avoid a PN-IP reset at the end of the ARM926 watchdog time.

Before the watchdog expires, an interrupt is generated for the ARM926 watchdog interrupt and the preliminary event 'WD_XWDOUT0' is signaled to the external host over a GPIO pin.

The watchdog also runs when the clock source fails (e.g. quartz break). In this case, the PLL switches to its free-running frequency (100 – 300 MHz).

When booting after a watchdog reset, the system uses the boot mode latched internally during PowerOn reset.

4.3.3.6 Asynchronous Software Reset for ERTEC 200P-3 (without PN-IP)

In the ERTEC 200P, an asynchronous software reset can be triggered by setting the 'RES_SOFT' bit in ASYN_RES_CRTL_REG; the PN-IP and PHYs are not reset. The SW_RES bit in RES_STAT_REG is set during an asynchronous software reset to allow an analysis of the reset event after a system restart. This bit is not affected by the reset function triggered. Upon restart, the software can read RES_STAT_REG.

When booting after a software reset, the system uses the boot mode latched internally during PowerOn reset.

4.3.3.7 Asynchronous Software Reset for PN-IP

The PN-IP and PHYs can only be reset asynchronously by the software with the 'RES_SOFT_PN' bit in the SCRB register 'ASYN_RES_CTRL_REG'.

The HW reset for the integrated PHYs is triggered by the 'phy_reset_o' output of the PN-IP. Whenever the SMI module in the PN-IP is not activated (configuration mode), 'phy_reset_o – output' is active and keeps the PHYs in the reset state.

A simultaneous asynchronous SW reset for the ERTEC 200P-3 and the PN-IP resets the complete ERTEC 200P.

4.3.3.8 Asynchronous Software Reset for the ARM926EJ-S Core

The ARM926EJ-S core (without TCM926) has its own reset, which can be executed asynchronously by the software with the 'RES_SOFT_ARM926_CORE' bit in the SCRB register 'ASYN_RES_ CTRL_REG'. 'RES_SOFT_ARM926_CORE' only affects the ARM926EJ-S core system and not TCM_Block_926. TCM_Block_926 is reset with XRESET, XSRST, XRES_ARM926_WD or RES_SOFT.

The SW_RES_ARM926 bit in RES_STAT_REG is set during an asynchronous software reset for the ARM926EJ-S core system to allow an analysis of the reset event after a system restart. This bit is not affected by the reset function triggered. Upon restart, the software can read RES_STAT_REG.

The asynchronous software reset for the ARM926EJ-S core system is needed once the boot loader has set the final TCM926 configuration. The TCM926 configuration (DRSIZE for D-TCM and IRSIZE for I-TCM → from TCM926_MAP register) is only applied to the ARM926EJ-S after a reset.

4.3.3.9 Synchronous Software Reset (PN-IP, PER-IF, XHIF)

The PN-IP, peripheral interface and host interface can be reset synchronously by the software in the SCRB register 'SYN_RES_CTRL_REG'. These synchronous resets affect the SYN reset inputs of the corresponding IPs and reset only the state machines and the local registers and not the parameter registers or the AHB interface. The synchronous reset does not affect the reset input of a flip-flop. The SW must set and then reset the relevant bits in 'SYN_RES_CTRL_REG'. This allows the SW to set the reset state itself.

4.4 GPIO Pins

The GPIO layer mainly provides means for flexible I/O pin mapping / routing. By use of multiplexers it is possible to obtain variable interconnections between predefined signal groups and ASIC I/O pins.

The structure of a single GPIO cell is shown in Figure 4-6. Each cell can either be used for I/O pin routing or as input / output pin of the GPIO parallel ports.

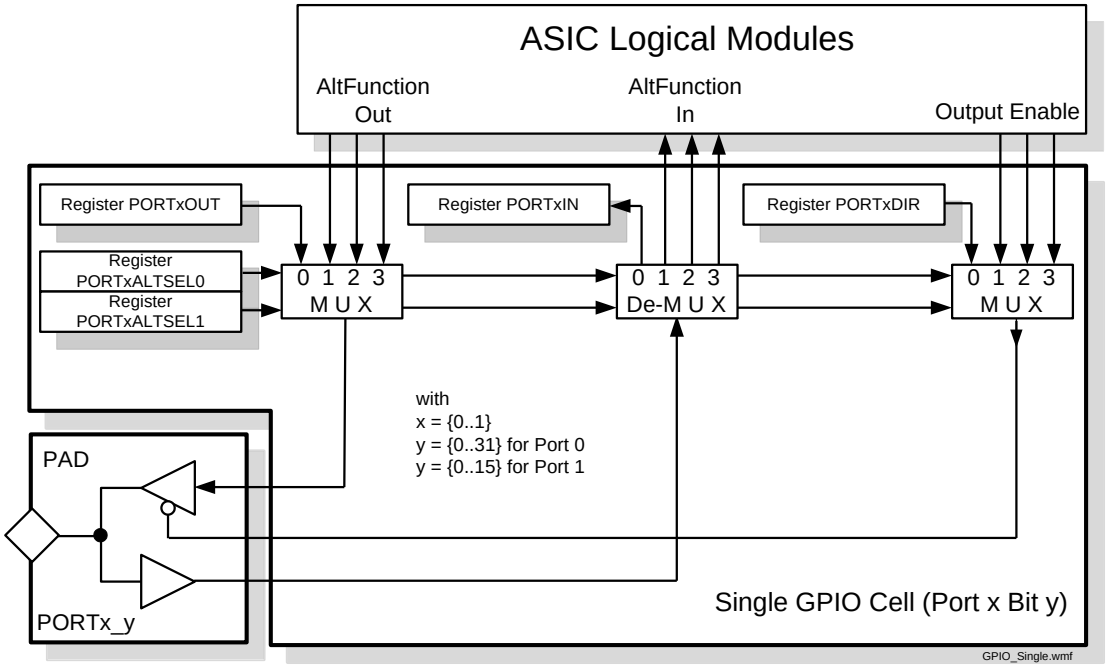

Figure 4-6: Single GPIO Cell

For I/O pin routing, one of 3 alternate functions can be selected for each GPIO cell. Also two parallel GPIO cells are used to provide 6 alternate functions for each GPIO (see chapter 4.6 for GPIO pin mapping).

4.5 Pull-up/down Resistors

See chapter 3.8.2

4.6 GPIO Pin Mapping

Table 4-5: GPIO Port 0 Input Mapping

GPIO Pin	GPIO Registers	GPIO Alternate Function A	GPIO Alternate Function B	GPIO Alternate Function C
GPIO0_INT	GPIO_*_0.0	PNPLL_OUT0_a	TIM_OUT0_a	reserved
GPIO1_INT	GPIO_*_0.1	PNPLL_OUT1_a	TIM_OUT1_a	reserved
GPIO2_INT	GPIO_*_0.2	PNPLL_OUT2_a	TIM_OUT2	DBGRQ
GPIO3_INT	GPIO_*_0.3	PNPLL_OUT3_a	TIM_OUT3	DBGACK
GPIO4_INT	GPIO_*_0.4	PNPLL_OUT4_a	TIM_OUT4	I2C_SDOI_1_a
GPIO5_INT	GPIO_*_0.5	PNPLL_OUT5_a	TIM_OUT5	I2C_SCLK_1_a
GPIO6_INT	GPIO_*_0.6	PNPLL_OUT6_a	TIM_TRIG0_a	I2C_SDOI_2_a
GPIO7_INT	GPIO_*_0.7	PNPLL_OUT7_a	TIM_TRIG1_a	I2C_SCLK_2_a
GPIO8_INT	GPIO_*_0.8	PNPLL_OUT8_a	TIM_TRIG2	SPI_2_SCLKIN_b
GPIO9_INT	GPIO_*_0.9	PNCLKA_IN_a	TIM_TRIG3	SPI_2_SFRMIN_b
GPIO10_INT	GPIO_*_0.10	NOT_USED	TIM_TRIG4	SPI_2_SSPOE_b
GPIO11_INT	GPIO_*_0.11	PNTIME_OUT_a	TIM_TRIG5	SPI_2_SSPCTLOE_b
GPIO12_INT	GPIO_*_0.12	PNTIME_IN	U2_CTS	SPI_2_SCLKOUT_b
GPIO13_INT	GPIO_*_0.13	WD_XWDOUT0_a	U2_RTS	SPI_2_SFRMOUT_b
GPIO14_INT	GPIO_*_0.14	I2C_SCLK_3	U2_TXD	SPI_2_SSPTXD_b
GPIO15_INT	GPIO_*_0.15	I2C_SDOI_3	U2_RXD	SPI_2_SSPRXD_b
GPIO16	GPIO_*_0.16	SPI_1_SCLKOUT_a	reserved	reserved
GPIO17	GPIO_*_0.17	SPI_1_SFRMOUT_a	reserved	reserved
GPIO18	GPIO_*_0.18	SPI_1_SSPTXD_a	reserved	reserved
GPIO19	GPIO_*_0.19	SPI_1_SSPRXD_a	reserved	reserved
GPIO20	GPIO_*_0.20	SPI_1_SSPOE_a	reserved	reserved
GPIO21	GPIO_*_0.21	SPI_1_SSPCTLOE_a	reserved	reserved
GPIO22	GPIO_*_0.22	SPI_1_SFRMIN_a	reserved	reserved
GPIO23	GPIO_*_0.23	SPI_1_SCLKIN_a	PNCLKA_IN_b	reserved
GPIO24	GPIO_*_0.24	SPI_2_SCLKOUT_a	TIM_OUT0_b	reserved
GPIO25	GPIO_*_0.25	SPI_2_SFRMOUT_a	TIM_OUT1_b	reserved
GPIO26	GPIO_*_0.26	SPI_2_SSPTXD_a	TIM_TRIG0_b	reserved
GPIO27	GPIO_*_0.27	SPI_2_SSPRXD_a	TIM_TRIG1_b	reserved
GPIO28	GPIO_*_0.28	SPI_2_SCLKIN_a	U3_TXD	PNTIME_OUT_b
GPIO29	GPIO_*_0.29	SPI_2_SFRMIN_a	U3_RXD	PNPLL_OUT6_b
GPIO30	GPIO_*_0.30	SPI_2_SSPOE_a	reserved	PNPLL_OUT7_b
GPIO31	GPIO_*_0.31	SPI_2_SSPCTLOE_a	reserved	PNPLL_OUT8_b

Table 4-6: GPIO Port 1 Input Mapping

GPIO Pin	GPIO Registers	GPIO Alternate Function A	GPIO Alternate Function B	GPIO Alternate Function C
XHIF_A1	GPIO_*_1.0	LOC_IO0	reserved	LOC_SCLKOUT0
XHIF_A2	GPIO_*_1.1	LOC_IO1	reserved	LOC_SFRMOUT0
XHIF_A3	GPIO_*_1.2	LOC_IO2	reserved	LOC_SSPTXD0
XHIF_A4	GPIO_*_1.3	LOC_IO3	reserved	LOC_SSPRXD0
XHIF_A5	GPIO_*_1.4	LOC_IO4	reserved	LOC_SCLKOUT1
XHIF_A6	GPIO_*_1.5	LOC_IO5	reserved	LOC_SFRMOUT1
XHIF_A7	GPIO_*_1.6	LOC_IO6	reserved	LOC_SSPTXD1
XHIF_A8	GPIO_*_1.7	LOC_IO7	reserved	LOC_SSPRXD1
XHIF_A9	GPIO_*_1.8	LOC_IO8	reserved	SPI_1_SCLKOUT_b
XHIF_A10	GPIO_*_1.9	LOC_IO9	reserved	SPI_1_SFRMOUT_b
XHIF_A11	GPIO_*_1.10	LOC_IO10	reserved	SPI_1_SSPTXD_b
XHIF_A12	GPIO_*_1.11	LOC_IO11	reserved	SPI_1_SSPRXD_b
XHIF_A13	GPIO_*_1.12	LOC_IO12	reserved	SPI_1_SSPOE_b
XHIF_A14	GPIO_*_1.13	LOC_IO13	reserved	SPI_1_SSPCTLOE_b
XHIF_A15	GPIO_*_1.14	LOC_IO14	reserved	SPI_1_SCLKIN_b
XHIF_A16	GPIO_*_1.15	LOC_IO15	reserved	SPI_1_SFRMIN_b
XHIF_A17	GPIO_*_1.16	LOC_IO16	reserved	U1_CTS
XHIF_A18	GPIO_*_1.17	LOC_IO17	reserved	U1_DCD
XHIF_A19	GPIO_*_1.18	LOC_IO18	reserved	U1_DSR
XHIF_SEG_2	GPIO_*_1.19	LOC_IO19	reserved	U1_RI
XHIF_SEG_0	GPIO_*_1.20	LOC_IO20	reserved	U1_RTS
XHIF_SEG_1	GPIO_*_1.21	LOC_IO21	reserved	U1_DTR
XHIF_XRDY	GPIO_*_1.22	LOC_IO22	reserved	U4_TXD
XHIF_XRQ	GPIO_*_1.23	LOC_IO23	reserved	U4_RXD
XHIF_XWR	GPIO_*_1.24	LOC_IO24	reserved	PNPLL_OUT0_b
XHIF_XRD	GPIO_*_1.25	LOC_IO25	reserved	PNPLL_OUT1_b
XHIF_XCS_R_A20	GPIO_*_1.26	LOC_IO26	reserved	PNPLL_OUT2_b
XHIF_XCS_M	GPIO_*_1.27	LOC_IO27	reserved	PNPLL_OUT3_b
XHIF_XBE0	GPIO_*_1.28	LOC_IO28	reserved	PNPLL_OUT4_b
XHIF_XBE1	GPIO_*_1.29	LOC_IO29	reserved	PNPLL_OUT5_b
XHIF_XBE2	GPIO_*_1.30	LOC_IO30	reserved	U1_TXD
XHIF_XBE3	GPIO_*_1.31	LOC_IO31	reserved	U1_RXD

Table 4-7: GPIO Port 2 Input Mapping

GPIO Pin	GPIO Registers	GPIO Alternate Function A	GPIO Alternate Function B	GPIO Alternate Function C
XHIF_D0	GPIO_*_2.0	LOC_IO32	reserved	reserved
XHIF_D1	GPIO_*_2.1	LOC_IO33	reserved	reserved
XHIF_D2	GPIO_*_2.2	LOC_IO34	reserved	reserved
XHIF_D3	GPIO_*_2.3	LOC_IO35	reserved	reserved
XHIF_D4	GPIO_*_2.4	LOC_IO36	reserved	reserved
XHIF_D5	GPIO_*_2.5	LOC_IO37	reserved	reserved
XHIF_D6	GPIO_*_2.6	LOC_IO38	reserved	reserved
XHIF_D7	GPIO_*_2.7	LOC_IO39	reserved	reserved
XHIF_D8	GPIO_*_2.8	LOC_IO40	reserved	reserved
XHIF_D9	GPIO_*_2.9	LOC_IO41	reserved	reserved
XHIF_D10	GPIO_*_2.10	LOC_IO42	reserved	NOT_USED
XHIF_D11	GPIO_*_2.11	LOC_IO43	reserved	WD_XWDOUT0_b
XHIF_D12	GPIO_*_2.12	LOC_IO44	reserved	reserved
XHIF_D13	GPIO_*_2.13	LOC_IO45	reserved	reserved
XHIF_D14	GPIO_*_2.14	LOC_IO46	reserved	reserved
XHIF_D15	GPIO_*_2.15	LOC_IO47	reserved	reserved
XHIF_D16	GPIO_*_2.16	LOC_IO48	reserved	I2C_SDOI_1_b
XHIF_D17	GPIO_*_2.17	LOC_IO49	reserved	I2C_SCLK_1_b
XHIF_D18	GPIO_*_2.18	LOC_IO50	reserved	I2C_SDOI_2_b
XHIF_D19	GPIO_*_2.19	LOC_IO51	reserved	I2C_SCLK_2_b
XHIF_D20	GPIO_*_2.20	LOC_IO52	reserved	reserved
XHIF_D21	GPIO_*_2.21	LOC_IO53	reserved	reserved
XHIF_D22	GPIO_*_2.22	LOC_IO54	reserved	reserved
XHIF_D23	GPIO_*_2.23	LOC_IO55	reserved	reserved
XHIF_D24	GPIO_*_2.24	LOC_IO56	reserved	reserved
XHIF_D25	GPIO_*_2.25	LOC_IO57	reserved	reserved
XHIF_D26	GPIO_*_2.26	LOC_IO58	reserved	reserved
XHIF_D27	GPIO_*_2.27	LOC_IO59	reserved	reserved
XHIF_D28	GPIO_*_2.28	LOC_IO60	reserved	reserved
XHIF_D29	GPIO_*_2.29	LOC_IO61	reserved	reserved
XHIF_D30	GPIO_*_2.30	LOC_IO62	reserved	reserved
XHIF_D31	GPIO_*_2.31	LOC_IO63	reserved	reserved

4.7 Configuration Pins

Global use cases and different test modes can be set with EMC pins that are latched in the CONFIG_REG register during an XRESET active PowerOn reset. These pins resume their EMC function in normal mode once the reset is cleared.

CONFIG(0): Enable REF_CLK output (25 MHz) or disable (tristate).

CONFIG(1): always ‘1’ - ARM clock 250 MHz.

CONFIG(2): always ‘0’ - The OSPI operates in Non-Oct-Mode

CONFIG(6-3): XHIF interface setting: (off, 16/32-bit)
XHIF_XRDY setting: (low-active, high-active)
XHIF_XWR setting: (Wr or Read/Write Control)

Table 4-8: Configuration Pins

CONFIG(6) **PIN: A23**	CONFIG(5) **PIN: A22**	CONFIG(4) **PIN: A21**	CONFIG(3) **PIN: A20**	CONFIG(2) **PIN: A19**	CONFIG(1) **PIN: A18**	CONFIG(0) **PIN: A17**	**Meaning**
-	-	-	-	-	-	**1**	REF_CLK tristate
-	-	-	-	-	-	0	REF_CLK output (25 MHz)
-	-	-	-	-	0	-	125 MHz ARM clock
-	-	-	-	-	**1**	-	250 MHz ARM clock
-	-	-	-	**0**	-	-	OSPI operates in Non-Oct-Mode
0	0	0	0	-	-	-	XHIF = on, 16-bit mode, GPIO95-80 and GPIO63-62 on (all inputs), XHIF_XWR has read/write control, XHIF_XRDY is high-active
0	0	0	1	-	-	-	XHIF = on, 16-bit mode, GPIO95-80 and GPIO63-62 on (all inputs), XHIF_XRD / XHIF_XWR separate, XHIF_XRDY is high-active
0	0	1	0	-	-	-	XHIF = on, 16-bit mode, GPIO95-80 and GPIO63-62 on (all inputs), XHIF_XWR has read/write control, XHIF_XRDY is low-active
0	0	1	1	-	-	-	XHIF = on, 16-bit mode, GPIO95-80 and GPIO63-62 on (all inputs), XHIF_XRD / XHIF_XWR separate, XHIF_XRDY is low-active
0	1	0	0	-	-	-	XHIF = on, 32-bit mode, GPIO95-32 off, XHIF_XWR has read/write control, XHIF_XRDY is high-active
0	1	0	1	-	-	-	XHIF = on, 32-bit mode, GPIO95-32 off, XHIF_XRD / XHIF_XWR separate. XHIF_XRDY is high-active
0	1	1	0	-	-	-	XHIF = on, 32-bit mode, GPIO95-32 off, XHIF_XWR has read/write control, XHIF_XRDY is low-active
0	1	1	1	-	-	-	XHIF = on, 32-bit mode, GPIO95-32 off, XHIF_XRD / XHIF_XWR separate, XHIF_XRDY is low-active
1	0	0	0	-	-	-	XHIF = SPI, GPIO95-62. 54-32 on (all inputs) **Note**: The boot code does **not** support an XHIF boot with the

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CONFIG(6) **PIN: A23**	CONFIG(5) **PIN: A22**	CONFIG(4) **PIN: A21**	CONFIG(3) **PIN: A20**	CONFIG(2) **PIN: A19**	CONFIG(1) **PIN: A18**	CONFIG(0) **PIN: A17**	**Meaning**
							setting CONFIG(6:3)="1000".
1	**0**	**0**	**1**	**-**	**-**	**-**	XHIF = off, GPIO95-32 on (all inputs)
1	1	0	0	-	-	-	XHIF = on, 32-bit mode, GPIO95-32 off, XHIF_XRD / XHIF_XWR separate, XHIF_XRDY is low-active, **Note:** The boot code does **not** support an XHIF boot with the setting CONFIG(6:3)="1100". If an XHIF boot is nevertheless necessary, it must be executed in the setting CONFIG_REG[6:3] == "0111".
Rest				-	-	-	XHIF = off, GPIO95-32 on (all inputs)

blue: Default setting with the internal pulls

Note

- GPIO configuration is done in hardware, XHIF configuration is done by PBL only if XHIF boot is selected
- During reset the internal pulls are not applied. External pulls must be connected in order to set the required settings.

4.8 Boot Pins

The required boot mode is saved in the BOOT_REG boot register. Some of the pins of the EMC interface are assigned to the boot register bits 0...4. The EMC pins are latched to the boot register during an active XRESET reset and return to their normal function with an inactive reset.

Table 4-9: Boot Modes

Boot(4) = XAV_BF	Boot(3) = A[16]	Boot(2) = A[15]	Boot(1) =XOE_DRIVER	Boot(0) = DTXR	Boot mode	Booting…	
1	1	0	0	1	**1**	External NOR flash (16-bit) [1], *ASYNC_ADDR_MODE* = 1	
1	**1**	**0**	**1**	**0**	**2**	External NOR flash (32-bit) [1], *ASYNC_ADDR_MODE* = 1	
1	1	1	1	1	**7**	XHIF full (external host	
0	1	1	1	0	**9**	Octal-SPI via external serial memory (slave)	8 Byte RSC [2]

[1] The secondary boot loader is run straight from the NOR flash and not from the TCM. The default mode, i.e., without external resistors, is a NOR flash with an access width of 32 bits and is selected with the internal pull circuit (highlighted in **blue**).

[2] With error correction and recognition (Reed-Solomon) of max. 8 bytes under usage of the Reed-Solomon Controller (RSC)

Note

During reset the internal pulls are not applied. External pulls must be connected in order to set the required settings.

4.8.1 Startup Times

Depending on the boot mode, the ERTEC 200P-3 requires one of the following startup times:

Table 4-10: Startup Times

Boot mode	Booting…		t_1	t_2 (startup time)
1	External NOR flash (16-bit), *ASYNC_ADDR_MODE* = 1	*Compile mode*	485 µs	n.a.[2)]
2	External NOR flash (32-bit), *ASYNC_ADDR_MODE* = 1	*Compile mode*	485 µs	n.a.[2)]
7	XHIF full (external host)		325 µs	41 µs per 1024 bytes (depends on external master speed)
9	Octal-SPI via external serial memory (slave)	8 bytes RSC [1)]	554 µs	454 µs per RSC page (236 bytes net), 515 µs for first RSC page

1) With error correction and recognition (Reed-Solomon) of max. 8 bytes under usage of the Reed Solomon Controller (RSC)

2 In Compile mode the SBL execution starts immediately after t_1. The SBL is executed by the processor directly from the source memory location (e.g., flash)

t_1: Time between XRESET end and loading of first SBL data.

t_2: Time from loading of first SBL data until the first command of the SBL is executed (startup time). This includes the time for copying data. If the alternative block is used or several data bytes are copied, the time may be longer.

The startup times in ERTEC 200P-3 are calculated based on $\mathbf{t_1+t_2}$.

5 Package

5.1 Package Drawing

The ERTEC 200P-3 has a 358-ball full grid P-LFBGA package. The ball pitch is 0.8 mm. The package size is 17 mm x 17 mm. The inner rows of balls act as the voltage supply and as thermal balls (see chapter 5.2).

Package dimensions
P-LFBGA358-1717-0.80-001/F01

"Unit:mm"

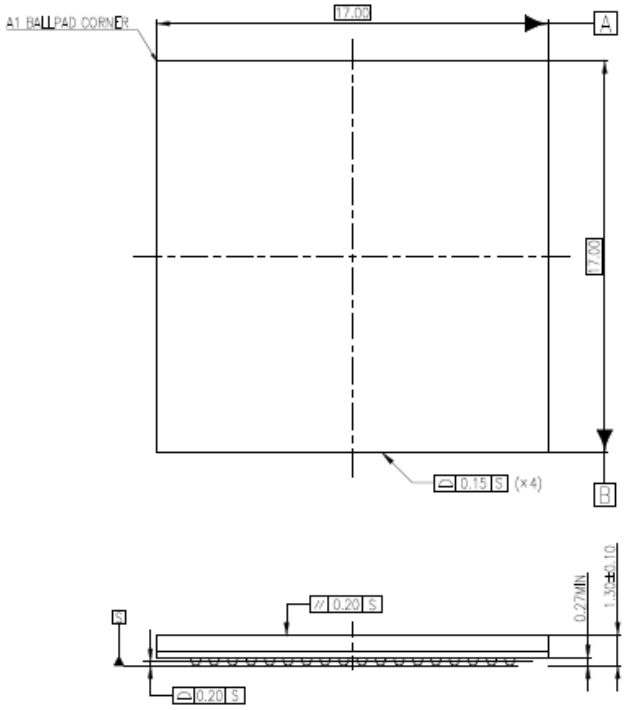
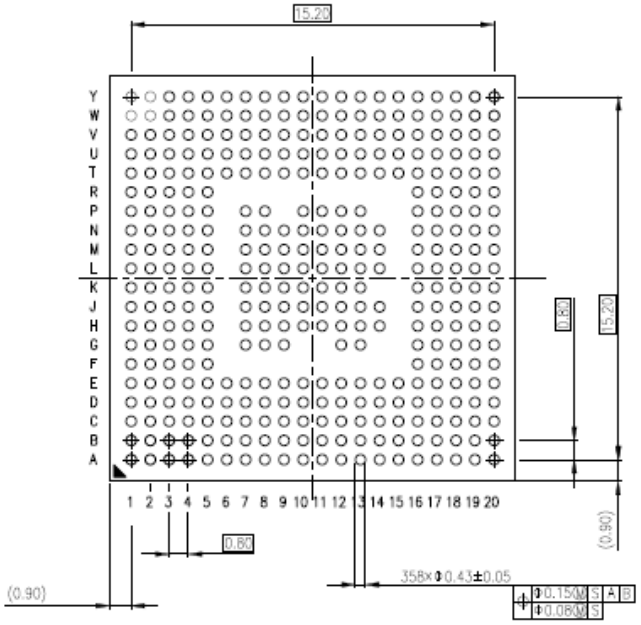


Figure 5-1: Package Dimensions (Top, Side)



Rev01

Figure 5-2: Package Dimensions (Bottom)

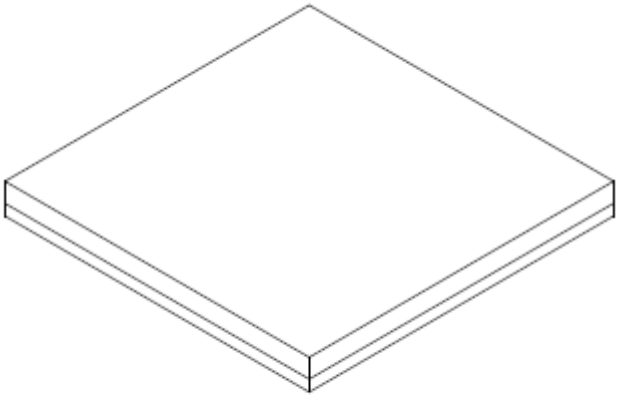


Figure 5-3: ERTEC 200P-3 Package Drawing

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5.2 Ball Layout

Top-View

Lower Ball	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	GND	GND	A_PHY_1	A_PHY_2	GPIO25	GPIO24	TMC2	REF_CLK	XTAL1	GND	GPIO12_INT	GPIO11_INT	GPIO18	GPIO7_INT	GPIO5_INT	TDI	TAP_SEL	D0	D13	GND
B	P2TDXN	P2TDXP	GND	GND	GPIO23	GPIO21	GPIO29	TACT	XTAL2	TEST	GPIO10_INT	GPIO14_INT	GPIO15_INT	GPIO6_INT	GPIO2_INT	RTCK	XTRST	D15	D4	D1
C	GND	GND	P2SDXN	P2SDXP	GND	GPIO27	GPIO20	GPIO26	GND	XSRST	GND	GPIO19	GPIO17	GND	GPIO0_INT	TDO	GND	D3	D2	D14
D	P2RDXN	P2RDXP	GND	GND	L_PHY_1	GPIO22	GPIO30	GPIO28	XRESET	GND	GPIO9_INT	GPIO13_INT	GPIO16	GPIO4_INT	GPIO1_INT	TCK	D11	D12	D9	D7
E	GND	GND	P2RXN	P2RXP	GND	L_PHY_2	GPIO31	GND	GND	GND	GPIO8_INT	BYP_CLK	TMS	GPIO3_INT	CHAIN_CTRL	GND	D6	DTXR	GND	D10
F	P2TXN	P2TXP	GND	GND	GND											GND	XOE_DRIVER	D8	XBE0_DQM0	XBE1_DQM1
G	GND	GND	P2FXEN	GND	GND		VDDIOA_PHY	VDD_CORE	VDD33			VDD33	VDD33			D5	XCS_PER1	XCS_PER0	A21	A22
H	XHIF_D2	XHIF_D15	GND	GND	GND		VDDIOD_PHY	VDDIOA_PHY	VSSIOA_PHY	GND	GND	VDD_CORE	GND	VDD_CORE		GND	A23	A18	A20	A17
J	XHIF_XRDY	XHIF_D10	XHIF_D13	XHIF_D6	VQPS		VDDA_PHY	VSSA_PHY	GND	GND	GND	GND	GND	VDD_EMC		A19	XWR	A15	GND	A16
K	XHIF_D5	GND	XHIF_D1	XHIF_D9	GND		AVDDHV_PLL	AVDD_PLL	GND	GND	GND	GND	VDD_CORE			XRD	XRDY_BF	A14	XAV_BF	XWE_SDRAM
L	XHIF_D8	XHIF_D7	XHIF_D14	XHIF_D11	GND		VDD_XHIF	VDD_CORE	GND	GND	GND	GND	GND	VDD_EMC		GND	CLK_O_SDRAM1	CLK_O_SDRAM2	XCAS_SDRAM	A13
M	XHIF_D4	GND	XHIF_D0	XHIF_D12	GND		VDDIOD_PHY	VDDA_PHY	VSSA_PHY	GND	GND	GND	GND	VDD_CORE		A12	XRDY_PER	A11	XRAS_SDRAM	XCS_SDRAM
N	XHIF_D3	XHIF_XBE1	XHIF_XBE0	XHIF_XIRQ	GND		VDDIOA_PHY	VSSIOA_PHY	GND	VDD_CORE	GND	GND	GND	VDD_EMC		CLK_I_SDRAM	A10	A0	GND	CLK_O_SDRAM0
P	GND	GND	P1FXEN	GND	GND		VDDIOA_PHY	VDD_CORE		VDD_XHIF	VDD_OSPI	VDD_OSPI	VDD_XHIF			A4	A6	A8	A9	A7
R	P1TXN	P1TXP	GND	GND	GND											GND	D16	XCS_PER3	A3	A1
T	GND	GND	P1RXN	P1RXP	GND	TMC1	XHIF_A19	XHIF_A18	GND	GND	XHIF_XBE3	XHIF_D30	XHIF_D24	GND	GND	GND	D29	A5	XBE2_DQM2	A2
U	P1RDXN	P1RDXP	GND	GND	XHIF_XWR	GND	XHIF_A15	GND	XHIF_A16	GND	XHIF_D21	XHIF_D28	XHIF_D29	XHIF_D20	XHIF_D17	D25	D17	XBE3_DQM3	GND	XCS_PER2
V	GND	GND	P1SDXN	P1SDXP	GND	XHIF_A12	XHIF_XCS_M	XHIF_A17	GND	GND	XHIF_A4	GND	XHIF_D27	GND	XHIF_D25	D21	D19	D27	D31	D18
W	P1TDXN	P1TDXP	GND	GND	XHIF_SEG_1	XHIF_SEG_2	XHIF_A10	XHIF_A9	XHIF_A3	XHIF_A1	XHIF_A2	XHIF_D31	XHIF_A14	XHIF_D18	XHIF_D16	GND	D26	D28	D30	D20
Y	GND	GND	XHIF_SEG_0	XHIF_XRD	XHIF_XCS_R_A20	XHIF_A13	XHIF_A11	XHIF_A6	XHIF_A7	XHIF_A5	XHIF_A8	XHIF_XBE2	XHIF_D26	XHIF_D22	XHIF_D23	XHIF_D19	D24	D23	D22	GND

Signals are grouped according to their color

Group
CLK/RES
TEST
JTAG
EMC
PN_PHY
L/A_PHY1/2
GPIO0…31
XHIF (GPIO32..55)

Figure 5-4: Ball Layout

5.3 Marking (Printed)

The ERTEC 200P-3 ASIC **package** is printed as follows:

Figure 5-5: Marking

5.4 Order Codes (MLFBs)

Table 5-1: Order codes

	Number of pieces[1]	Order Code	Packing information
ERTEC200P-3	10	6ES7195-0BH03-0XA0	Cut Tape
ERTEC200P-3	100	6ES7195-0BH13-0XA0	Tape&Reel
ERTEC200P-3	800	6ES7195-0BH33-0XA0	Tape&Reel

5.5 Thermal Characteristics

The following values apply to the ERTEC 200P-3 through usage of the selected package:

Table 5-2: Thermal Characteristics

Package	Ambient temperature T_A	junction-to-ambient air thermal resistance θ_{ja}	junction-to-top thermal characterization parameter Ψ_{jt}
P-LFBGA358-1717-0.8 (ERTEC 200P-3)	25 °C	27.9 °C/W	0.32 °C/W
	85 °C	24.5 °C/W	0.35 °C/W

The conditions are as follows:

- Chip size 3.962 mm x 4.592 mm
- Natural air cooling (no airflow)
- JEDEC standards conformance
- Six layer board (thickness 1.2 mm, layer stack A5E00886630BS, 85% VIA/Ball)

[1] The number of pieces may be subject to change.

- Thermal resistance around the working point of 1.1 W

With

T_T … temperature at the top center of the package and

P … the chip's total power dissipation

The ERTEC 200P-3 junction temperature T_J can be estimated with formulas (1) or (2).

(1) $\theta_{ja} = (T_J - T_A) / P$
(2) $\Psi_{jt} = (T_J - T_T) / P$

EIA/JEDEC51-1, 51-2 define thermal characters as follows,

θ_{ja} Thermal resistance, junction-to-ambient

Ψ_{jt} Thermal characterization parameter, junction to the top center of the package surface.

θ_{jc} Thermal resistance, junction-to-case

θ_{jb} Thermal resistance, junction-to-ball

5.5.1 Max. junction temperature T_J

With a maximum power dissipation of the ERTEC 200P-3 of **< 944 mW** (see chapter 3.9) an actual junction temperature (temperature on the die) results of:

Table 5-3: Max. Juction Temperature

	Ambient temperature T_A	**Junction temperature T_J**	**Top-Case temperature T_T**
P-LFBGA358-1717-0.8 (ERTEC 200P-3)	**25°C**	< 51.4 °C	< 51.1 °C
	85°C	< 108.2 °C	< 107.8 °C

The lifetime depends on the junction temperature at 100 % duty.

Table 5-4: Livetime

Junction Temperature (with 100% duty)	**Hard Error FIT Rate**	**Max. Lifetime**[1]
100°C	4.4 FIT	10 years
105°C	5.9 FIT	10 years
108°C	7.0 FIT	10 years
110°C	7.8 FIT	10 years
112°C	8.7 FIT	10 years
115°C	10.2 FIT	7.7 years
118°C	12.0 FIT	6.1 years
120°C	13.3 FIT	5.3 years

5.6 Solder Profile

The following lead-free reflow soldering profile (acc. to the IPC J-STD-020D-1) will be guaranteed.

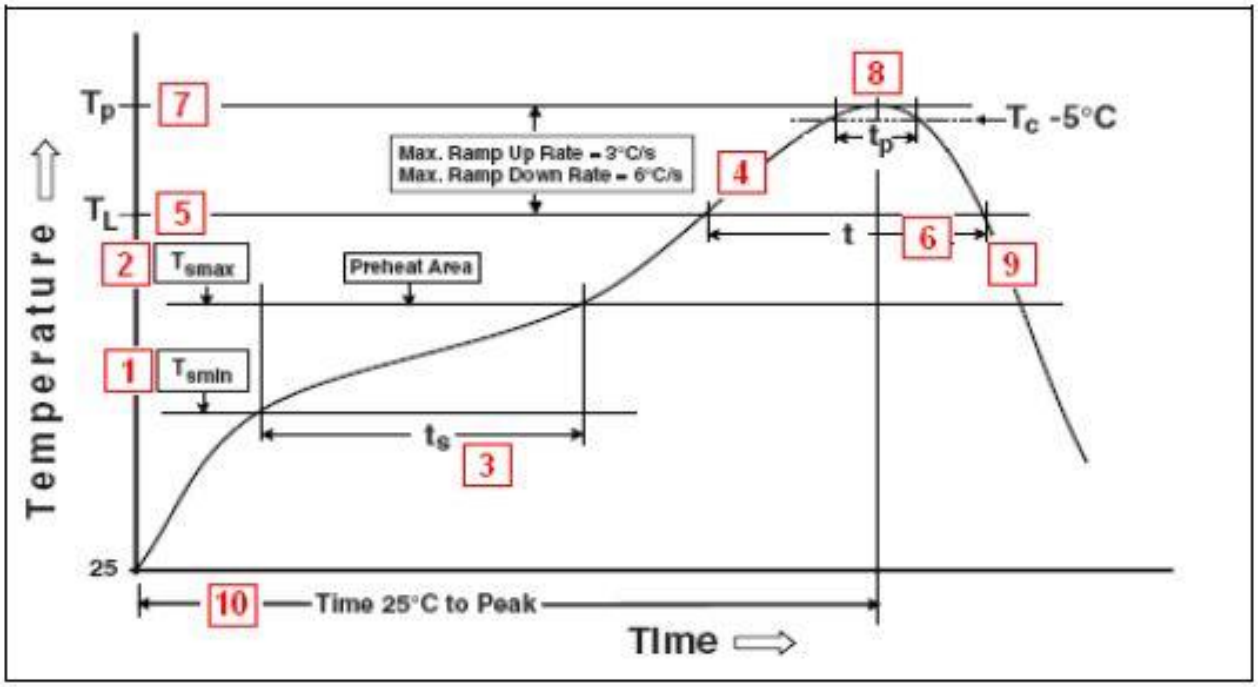

Figure 5-6: Solder Profile

[1] After this period of time the devices will fail epidemically because of electromigration. The values of the maximum lifetime for a junction temperature below 112°C shall be higher than 10 years, but Toshiba supports a maximum of 10 years for this technology only. The devices, which are used at these lower temperatures, will not fail after 10 years epidemically.

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Table 5-5: Tabular form for soldering profile data

Key	Par.	Profile Feature	Pb free Process
R.1	T_{smin}	Minimum pre-heating temperature	150 °C
R.2	T_{smax}	Maximum pre-heating temperature	200 °C
R.3	t_s	Pre-heating time (T_{smin} to T_{smax})	120 sec
R.4	dT/dt up	Average ramp-up rate (T_{smax} to T_p)	3 °C/sec max.
R.5	T_L	Liquidous temperature	217 °C
R.6	**t_L**	**Time duration at liquidous**	**min. 90 sec**
R.7	T_p	Peak package body temperature	min. 260°C for package < 350 mm^3
			min. 245°C for package > 350 mm^3
R.8	t_p	Time within 5 °C of the specified Peak package body temperature T_p	min. 30 sec
R.9	dT/dt down	Average ramp-down rate (T_p to T_{smax})	6 °C/sec max.
R.10	$t_{25°\text{-peak}}$	Time 25 °C to peak temperature	8 minutes max.

Measurement points during re-flow soldering: at the critical termination, the top side of the component body (acc. to the IEC 60068-2-58). Number of passes: all products supporting reflow soldering shall be capable of 3 passes.

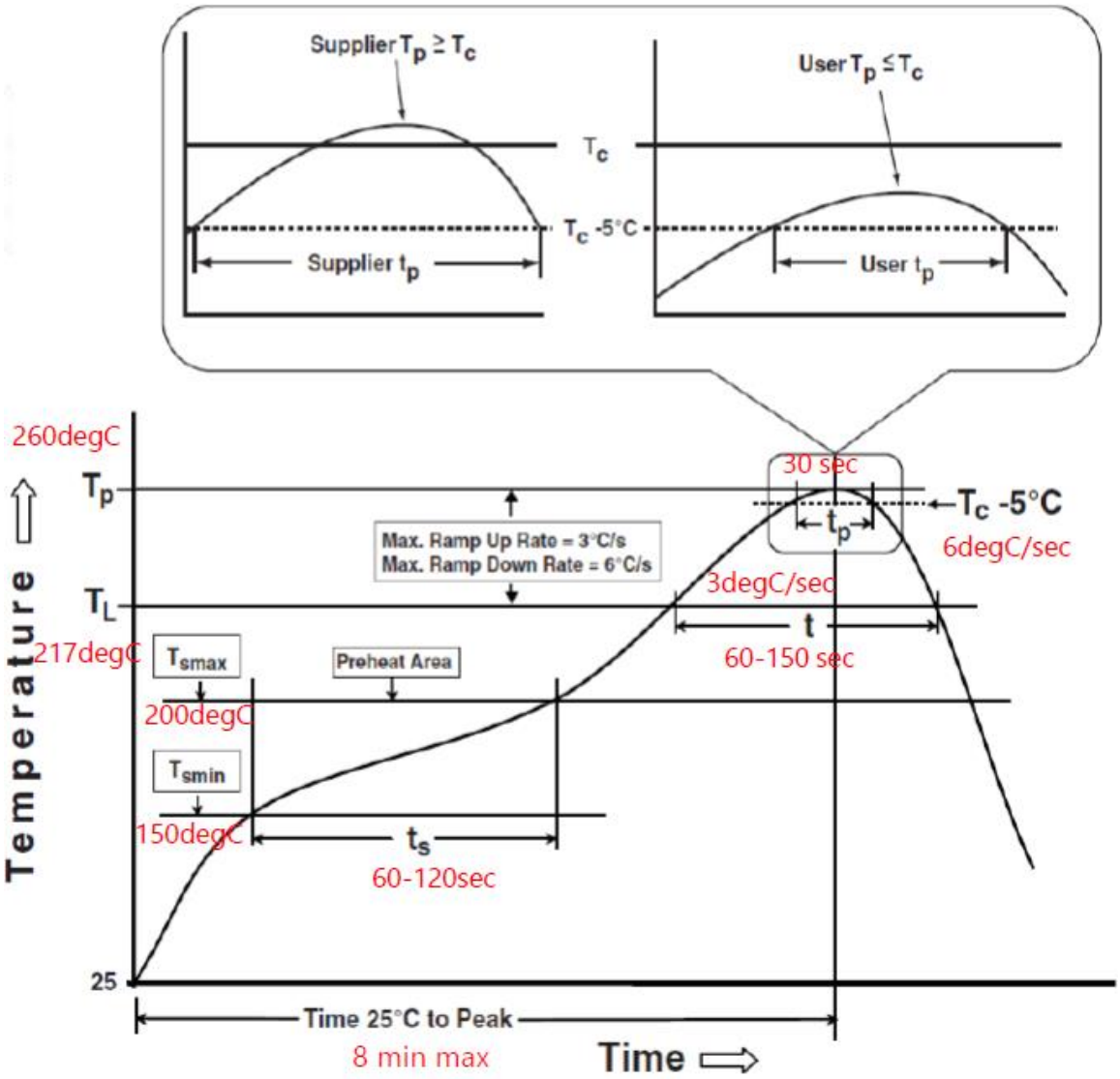

Figure 5-7: Reflow Profile

Table 4-2 Pb-Free Process – Classification Temperatures (T_c)

Package Thickness	Volume mm³ <350	Volume mm³ 350 - 2000	Volume mm³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

5.7 Packing Information

5.7.1 Tape&Reel

Final testing and packing will be done at two different sites (STK in Oita/Japan and ASE in Kaohsiung/Taiwan). The Tape&Reel specification differs slightly.

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5.7.1.1 Tape&Reel specification for STK final testing and packing

Toshiba product name: T6WZ9SBG-0001(ETO)

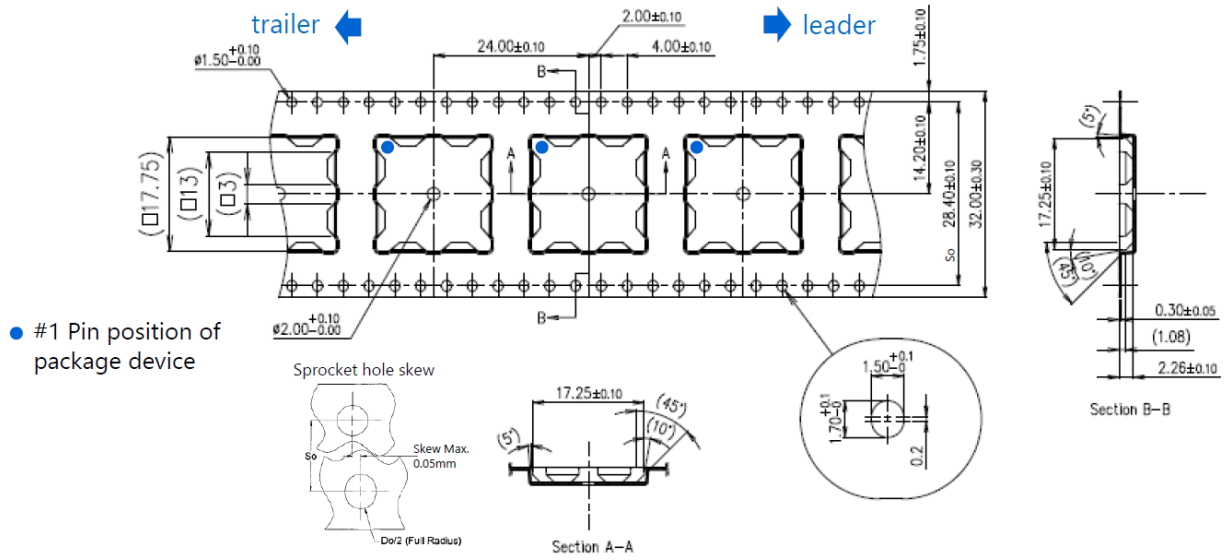


Figure 5-8: Carrier Tape (STK)

Note

The corner and ridge radiuses (R) of inside cavity are 0.3 mm max.

Cumulative tolerance of 10 pitches of the sprocket hole is ±0.2 mm.

Measuring of cavity positioning is based on cavity center in accordance with JIS/IEC standard.

Carrier tape dimensions follow EIA-481 standard.

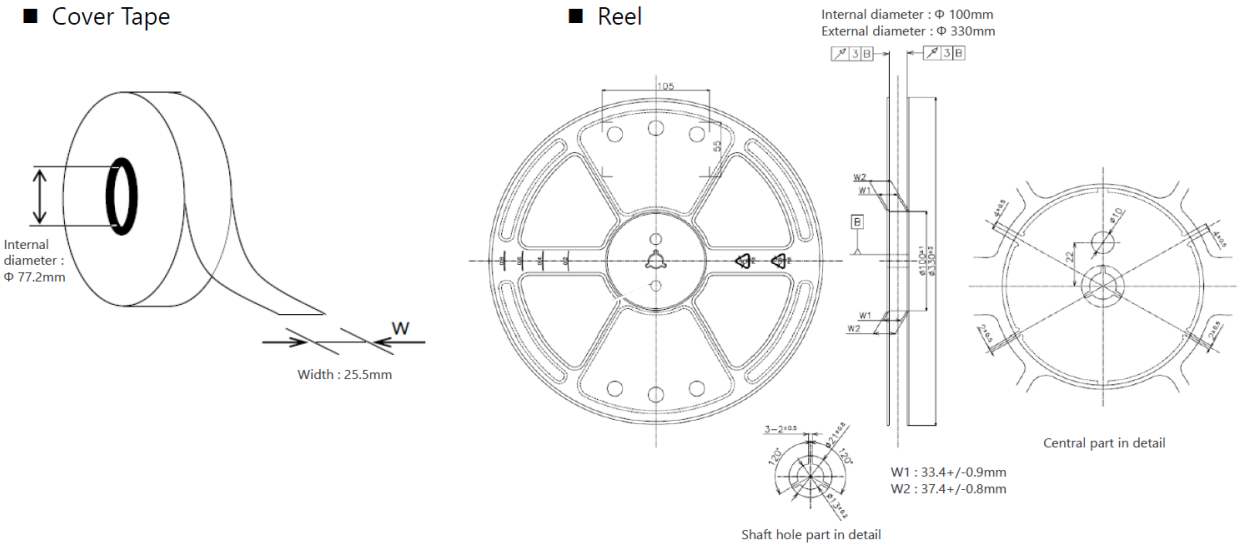


Figure 5-9: Cover Tape & Reel (STK)

5.7.1.1 Tape&Reel specification for ASE final testing and packing

Toshiba product name: T6WZ9SBG-0001(ETT)

■ **Carrier Tape**

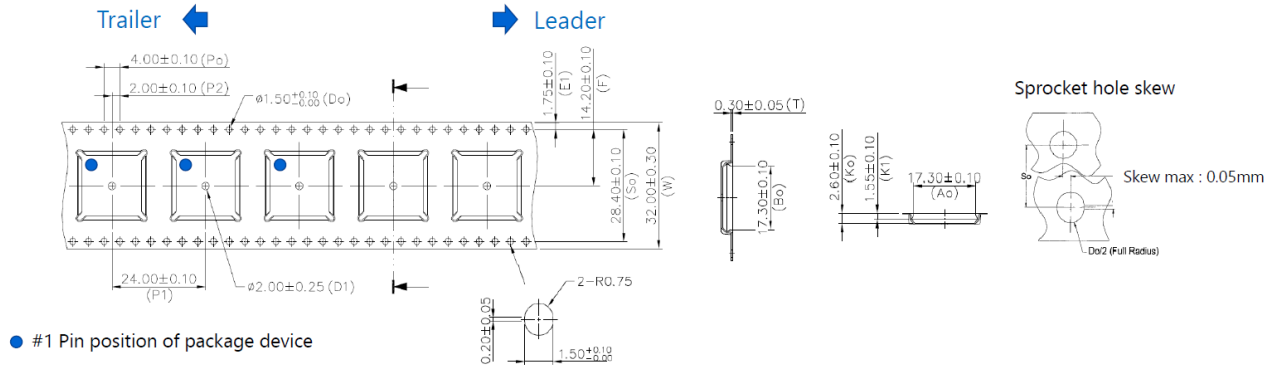


Figure 5-10: Carrier Tape (ASE)

Note

Carrier tape dimensions follow EIA-481 standard.

Dimensions in mm.

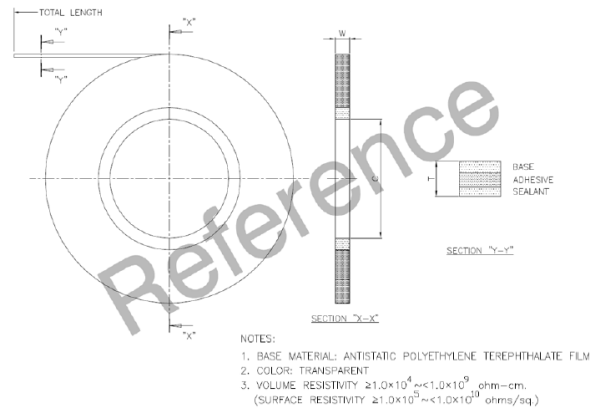
10 Sprocket hole pitches cumulative tolerance ±0.20 mm.

Camber not to exceed 1 mm in 250 mm.

Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

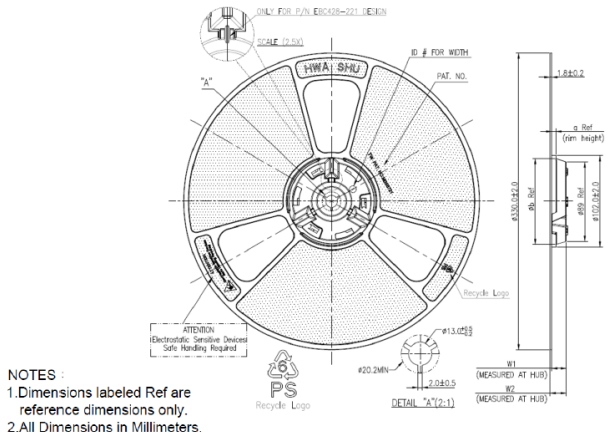
Volume resistivity ≥ 1.0*10^4 ~ <1.0*10^{11} ohm-cm (surface resistivity ≥ 1.0*10^5 ~ <1.0*10^{12} ohms/sq

■ **Cover Tape**



C	T	W
76.6mm	0.052(+/-0.005)mm	25.5(+/-0.1)mm

■ **Reel**



Normal Hub Width	W1	W2 max	a	b
16mm	16.5(+0.70/-0.30)	19.2	4.5	96

Figure 5-11: Cover Tape & Reel (STK)

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5.7.2 Packing

5.7.2.1 Packing specifications for STK final testing and packing

Figure 5-12: Packing specifications (STK)

5.7.2.2 Packing specifications for ASE final testing and packing

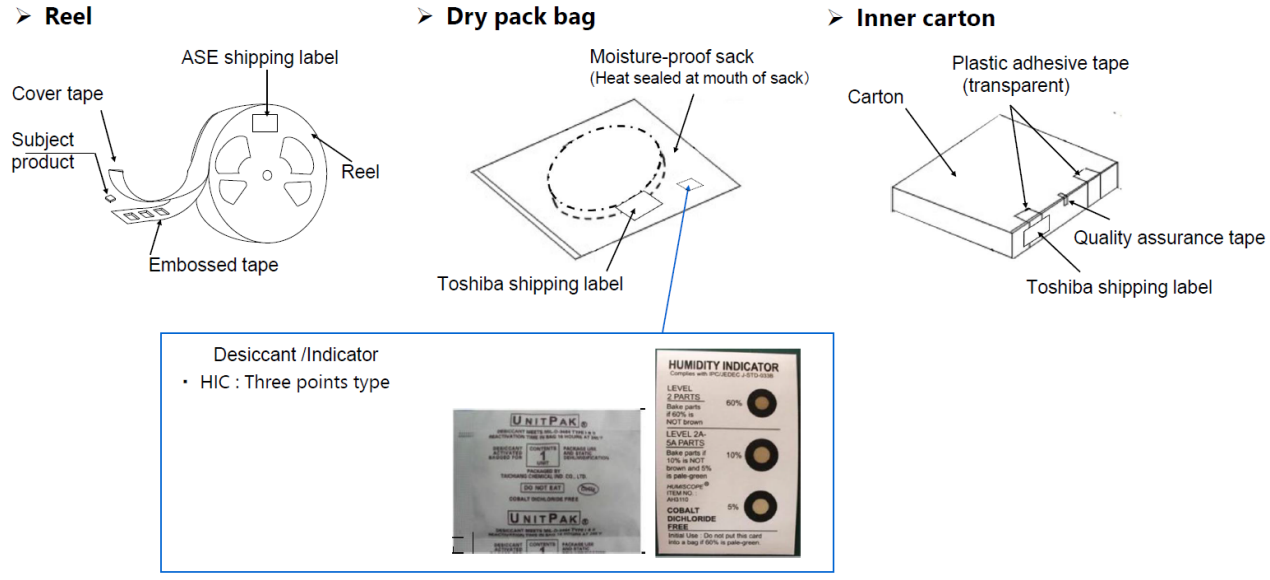

Figure 5-13: Packing specification (ASE)

5.7.3 Moisture Sensitivity Level

ERTEC 200P-3: J-STD-20 MSL3.

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5.7.4 Storage Temperature

Table 5-6: Storage Temperature

	symbol	min		max	unit
Storage Temperature	Tstg	-40		125	°C

6 Quality

6.1 Hard-Error FIT Rates

(24h per day and 60% UCL (Upper Confidence Level))

Table 6-1: Hard-Error FIT Rates

	FIT-Rate for hard errors / silicon defects:
60°C ambient temperature	1.8 FIT (in 10 years), Component Hours (Device hour): 1.13E+09 hr
70°C ambient temperature	3.3 FIT (in 10 years), Component Hours (Device hour): 8.30E+08 hr
85°C ambient temperature	7.8 FIT (in 10 years), Component Hours (Device hour): 2.58E+08 hr

6.2 Soft-Error FIT Rates

Double bit errors: The adjacent bits in single port RAMs are in different words, therefore they can be corrected by ECC. Based on literature values and simulation results double bit fails have a probability of 1/10th to 1/100th of single bit fails.

Soft-error rate for the memories in the ERTEC 200P-3 (alpha & neutron):

Table 6-2: Soft-Error FIT Rates

	0m	2000m	2300m	2500m	3000m	3500m	4000m	5000m
Alpha[1]	16.1 FIT							
Neutron[2]	33.5 FIT	176.2 FIT	220.1 FIT	254.3 FIT	359.8 FIT	500.5 FIT	684.4 FIT	1220.1 FIT
Factor to neutron 0m[3]	*x 1.0*	*x 5.26*	*x 6.57*	*x 7.59*	*x 10.74*	*x 14.94*	*x 20.43*	*x 36.42*
Total SER	**49.6 FIT**	**192.3 FIT**	**236.2 FIT**	**270.4 FIT**	**375.9 FIT**	**516.6 FIT**	**700.5 FIT**	**1236.2 FIT**

Note

The neutron factor for various different heights can be calculated at the following WEB link: http://www.seutest.com/cgi-bin/FluxCalculator.cgi

6.3 RoHS / REACH

Information about RoHS and REACH can be found at BOMcheck (see https://app.bomcheck.com/) with the Toshiba product name: T6WZ9SBG.

[1] Calculation based on 175 FIT/MBit

[2] Calculation based on 364 FIT/MBit

[3] Location: New York, USA

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